ULTRA-LOW DIELECTRIC CONSTANT AND ULTRA-THIN POLYMER DIELECTRIC MATERIALS, PROCESSES AND RELIABILITY FOR ULTRA-HIGH BANDWIDTH COMPUTING APPLICATIONS

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Materials Science and Engineering

Georgia Institute of Technology
May 2020

ULTRA-LOW DIELECTRIC CONSTANT AND ULTRA-THIN POLYMER DIELECTRIC MATERIALS, PROCESSES AND RELIABILITY FOR ULTRA-HIGH BANDWIDTH COMPUTING APPLICATIONS

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To my parents

ACKNOWLEDGEMENTS

I'm extremely grateful to Prof. Rao Tummala, my advisor for giving me the opportunity to be a part of the Georgia Tech Packaging Research Center (GT-PRC), for his vision and drive and for teaching me to problem-solve with an 8-step structure. I would like to thank my co-advisor Prof. Mark Losego, for his support and passion for research, and for teaching to perform and communicate quality research. I am very grateful to Prof. Raj Pulugurtha, for his constant support, patience, encouragement, guidance and mentorship, I've learnt a lot working with him over the years. I would also like to thank my committee members Prof. C P Wong and Prof. Natalie Stingelin, for their valuable inputs, time and encouragement of my work.

I would like to thank all the visiting engineers at GT-PRC for discussions and assistance, their critical inputs have helped me design experiments better and quantify outcomes of value to the industry. I'd like to particularly thank Dr. Atsushi Kubo (TOK), Takenori Kakutani (Taiyo), Daichi Okamoto (Taiyo), Kimiyuki Kanno (JSR) and Dr. Amit Agarwal. I would also like to thank the team at Intel for valuable discussions. Further, I'm grateful to everyone who's trained me in the cleanroom and characterization facilities. I'm extremely grateful to all the PRC research engineers, PRC and Losego lab students and interns who've helped me in this thesis, particularly Dr. Chandra Nair for training and useful discussions, Dr. Fuhan Liu, for always having an open door to talk to, Dr. Vanessa Smet for her constant encouragement and support, Dr. Venky Sundaram, for providing opportunities to interact closely with industry partners, Prof. Swaminathan for his support of this thesis, Dr. Mohan Kathaperumal, for reviewing my thesis document, Siddharth Ravichandran, for support in electrical design and constructive discussions, Bartlet DeProspo and Pratik Nambiar, for fabrication support and useful discussions, Jenefa Kannan, for fabrication support on BCB, Neha Kondekar, for developing the in-situ XPS study,

Emily McGuinness, for help with Adobe Illustrator. I'm extremely grateful to all the Losego lab members who've built and maintained the VPI reactors that I was able to use. I'd also like to thank my office mates, Atom Watanabe and Dr. Timothy Huang for interesting discussions on fabrication and coffee.

I'd like to thank my friends for fun, laughter, food and random conversations, for always being up for playing badminton and for being my family in Atlanta. Finally, I would like to thank my parents, for their unconditional support and for always encouraging me to dream big.

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LIST OF ABBREVIATIONS

BCB	Benzocyclobutene
BEOL	Back end of line
CMP	Chemical mechanical polishing
CTE	Coefficient of thermal expansion
CVD	Chemical vapor deposition
DoE	Design of experiments
D_k	Dielectric constant
DoP	Degree of Planarization
ENIG	Electroless nickel, immersion gold
FC	Fluropolymer
FEM	Finite element modeling
FTIR	Fourier transform infrared spectroscopy
HAST	Highly accelerated stress test
I/O	Input and Output
PCB	Printed circuit board

PI	Polyimide
PID	Photo imageable dielectric
RDL	Re-distribution layer
SAP	Semi-additive processes
SEM	Scanning electron microscopy
TCT	Thermal cycling test
T_g	Glass transition temperature
TSR	Total strain range
TTV	Through thickness variation
WLP	Wafer level packaging
XPS	X-ray photoelectron spectroscopy

SUMMARY

The increase in the number of connected devices in homes, cars and offices coupled with the growth of advanced data processing algorithms enabled by artificial intelligence (AI) has been driving an unprecedented need for ultra-high bandwidth computing. At the package level, the bandwidth increase can be achieved by increasing the number of input-output (I/O) connections or by increasing the data rate for each connection. The number of I/Os depends on the wiring density supported by each layer and the number of layers. These layers must be vertically spaced at ultra-small distances to enable high-wiring density. The data rate is primarily influenced by the dielectric constant or D_k. Hence, the focus of this research is to develop ultra-low D_k and ultra-thin polymer dielectric materials, processes and reliability to meet the next-generation computing needs of ultra-high bandwidth.

Silicon back-end-of line (BEOL) wiring has significant limitations such as high RC delays because of the choice of dielectric materials and cost and thus, is challenged in meeting bandwidth requirements. Current organic materials and processes are limited by their incapacity to scale to fine features because of thick dielectric materials and poor dimensional stability of the core. This research is focused on addressing the limitations of current approaches and demonstrating the potential for ultra-low D_k, ultra-thin polymer dielectrics to signal at higher data rates, process guidelines for panel-scalable and low-cost processes and investigates the reliability of ultra-thin, ultra-low D_k dielectrics, thus leading to enhanced electrical performance and lower cost compared to silicon BEOL and current organic RDL.

The specific objectives of this thesis are to a) develop ultra-low-D_k (< 3.0) and ultra-thin (2-5 μm) polymer dielectric materials with optimal properties for high-signal speed, b) develop

panel-scale processes for ultra-thin dielectrics with high surface planarity capable of supporting fine line/spaces of < 2 µm line width/space and < 5 µm diameter vias and, c) investigate the thermo-mechanical and chemical reliability of polymer/copper interfaces .

In summary, this thesis explores polymer materials classes in their compatibility for RDL wiring in terms of their material properties, ease of fabricating fine-pitch features on planar and smooth surfaces and finally, in creating reliable copper/polymer interfaces with good adhesion

CHAPTER 1. INTRODUCTION

The primary motivation of this research is to develop ultra-low D_k and ultra-thin polymer dielectric materials, processes and reliability capable of meeting next-generation interconnection needs for re-distribution layer (RDL) wiring to achieve ultra-high bandwidth. The specific objectives of the research performed are:

1. Materials – Develop ultra-low-D_k (<3.0), ultra-thin polymer dielectric materials with the optimal electrical, mechanical, chemical and physical properties

2. Processes – Develop ultra-thin (2- 5 μm) panel processes to achieve planar ultra-thin dielectrics for high-density RDL wiring

3. Reliability – Study the thermo-mechanical and chemical reliability of ultra-low D_k, ultra-thin RDL dielectric materials

The increase in the number of connected devices in homes, cars and offices coupled with the growth of advanced data processing algorithms enabled by artificial intelligence (AI) has been driving an unprecedented need for ultra-high bandwidth computing. This need for ultra-high bandwidth is driving transistor density on single-chips, which is in turn is driving the requirement for ultra-high wiring density and input-output connections (I/O_s) at small interconnection bump pitches on the package side. While these characteristics have been well developed on the chip-level, they are not achieved at the package level. Bandwidth is driven by two factors—number of I/Os and the bit rate per I/O, while the number of I/O_s are determined by the wiring density and the number of layers; the bit rate is determined by signal speed and interconnect length. Signal speed is determined primarily by the dielectric constant. Figure 1 summarizes the key drivers for ultra-high bandwidth.

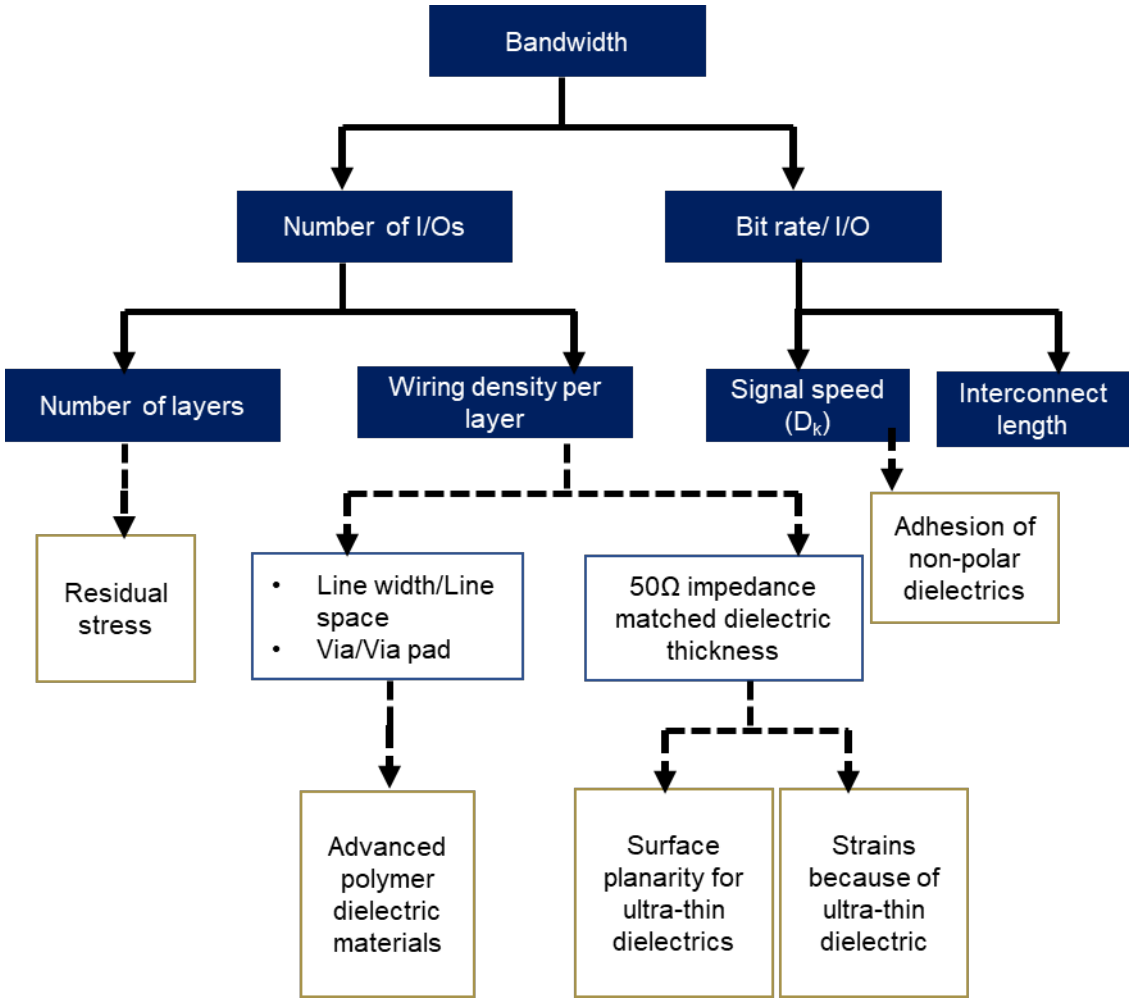


Figure 1 Drivers for Ultra-high bandwidth

The electrical property of the dielectric material that controls the signal speed is the dielectric constant (D_k). The critical challenge is to develop polymer materials with all the other required properties. This is one of the tasks of this dissertation, of developing ultra-low D_k dielectric materials.

Achieving high wiring density requires multiple layers of re-distribution layer (RDL) wiring with ultra-small line widths at ultra-small spaces and ultra-small via diameters as shown in Figure 1. In addition, the multiple wiring layers must be spaced in a vertical direction close enough such that a 50 Ω characteristic impedance is maintained. This 50 Ω impedance is considered an optimal value for achieving

low loss and good power handling. The characteristic impedance is calculated with the equation given below for a microstrip line:

$$Zo = \frac{120\pi}{\sqrt{\varepsilon_{eff}}(1.393 + \frac{W}{H} + \frac{2}{3}\ln\left(1.44 + \frac{W}{H}\right))} \quad (1)$$

where ε_{eff} is the effective dielectric constant of the microstrip line, and W/H is the ratio of line width to height (or thickness) of dielectric. As can be seen, the dielectric constant is inversely proportional to the dielectric height which means that for a 2 μm line width of conductor which is the focus of this thesis work, the dielectric thickness needs to be ~2 μm for an ultra-low D_k material. This requires optimization of processes to ensure that the dielectric height can be maintained for a 50 Ω impedance match. Thus, the second objective of the proposed research includes developing panel-scale processes for ultra-fine-pitch features using ultra-thin dielectrics.

As the wiring density scales to finer pitches, it becomes challenging for the copper lines to stick to the dielectric. This problem is further aggravated by the choice of ultra-low D_k dielectric material which inherently is non-polar/hydrophobic and does not have adequate bonding groups for chemical bonding with an adhesion layer. Further, ultra-thin dielectric materials increase the aspect ratio for microvias thereby increasing the overall strains in the microvia/pad interface. This can lead to copper cracking Hence, the third objective of this proposed research is to investigate the reliability of polymer/copper interfaces with ultra-thin, ultra-low D_k polymer dielectrics.

In addressing the barriers stated above, this thesis investigates polymer materials classes in their compatibility for RDL wiring in terms of the material properties, ease of fabricating fine-pitch features

along with planar and smooth surfaces and finally, in creating reliable copper/polymer interfaces with good adhesion. Thus, this thesis focuses on developing ultra-low D_k, ultra-thin polymer dielectric materials, processes and reliability to meet the needs of ultra-high bandwidth for next-generation high-performance computing.

Advanced packaging offers an attractive opportunity to continue scaling from a systems-level rather than a transistor-level and continue to extend the same scaling and functionality benefits such as signal speed and enable "More than Moore" scaling. Systems-scaling looks at putting together heterogeneous chips (chips designed for different functions such as RF or logic chips) and interconnecting them. The System-on-Package (SoP) concept pioneered by Prof. Rao R. Tummala at GT and others as a methodology to integrate all system functions with seamless interaction in a single package to enable system-scaling [1]. SoP can be used to integrate multiple functions such as digital, RF, sensors and optical in a single package serving diverse application areas such as MEMS (micro-electromechanical systems), mobile and other consumer devices. The primary goal of a system is to enable maximum data throughput between the chips. There are new packaging architectures being developed to support heterogeneous integration and tackle the information exchange between chips by increasing the number of I/Os while the power at its lowest level. These architectures include planar 2D structures such as interposers where chips are placed next to each other or 3D architectures where chips are stacked on top of each other. The drive towards higher I/O density in these architectures is enabled by the package substrate technology which serves to provide wiring between chips and to the board. While package substrates have evolved from thick film substrates which are made of ceramics with co-fired dielectric layers to thin-film based organic substrates with thin polymer dielectrics and silicon-based substrates with spin-on polymers, the focus of this work is on the re-distribution layer (RDL) wiring which interconnects the chips on the package substrate. The RDL consisting of multi-layers of conductors and insulators is the most value-added part of the package

substrate because it serves to interconnect dies. Signal delay in global interconnects on ICs dominates gate delay as the process node is reduced, with this work, ultra-low D_k dielectrics on advanced package substrates offers a unique opportunity for the global wiring to be off-loaded to the substrate RDL and maintain high-signal speed. Today, the main challenge in packaging is however, not simply to develop materials with the lowest dielectric constant but to find materials that satisfy all the electrical, physical, mechanical and chemical properties and can be processed at low-cost. The primary goal of this thesis is to therefore develop ultra-low-D_k, ultra-thin polymer dielectric materials with optimal properties, develop processes for RDL fabrication and evaluate the reliability of these materials.

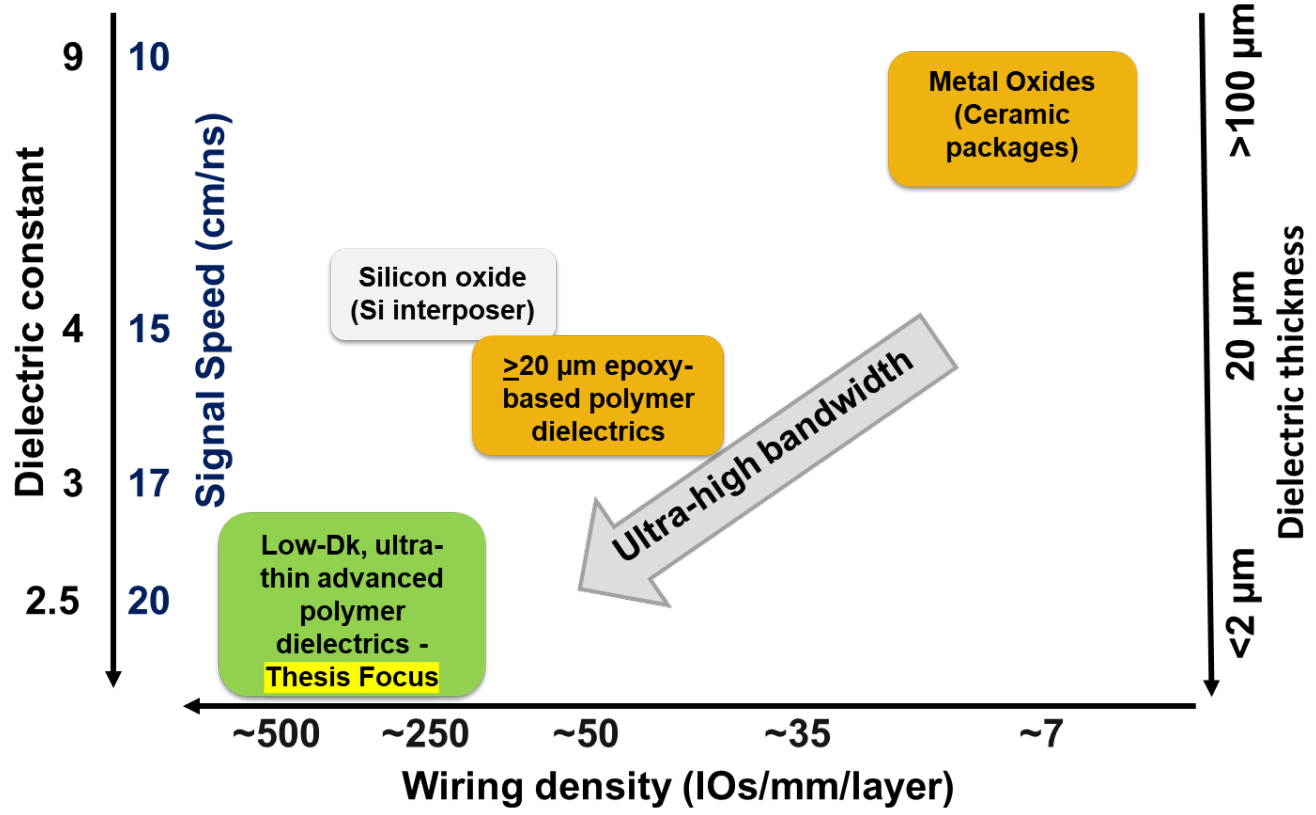


Figure 2 Strategic need to move towards ultra-low D_k (<3.0), ultra-thin dielectrics for ultra-high bandwidth

1.1 Historic evolution of ultra-low D_k and ultra-thin polymer dielectric materials

Polymers enable multiple aspects of the package. Typically, most polymers used in packaging are thermosets which means that during processing a chemical reaction transforms small molecules into a large cross-linked network. Most of these polymers are resins formulated with high performance fillers to achieve specific required material properties. The first lead frame package was called "dual-in-line" packaging or DIP where two rows of lead fingers soldered into plated through holes on the circuit board are surface mounted. The lead frame is wire bonded (gold or copper wire is attached from the bond pad on the top of the chip to the lead finger) to the die and then overmolded using an epoxy molding compound which protects the chip from mechanical damage and reduces moisture diffusion into the package. This is an early example of polymers used in packaging with a thickness >1 mm. Packaging technology evolved to surface mount components (SMT) with peripheral lead fingers and then to grid array type packages where the substrate was used to "fan-out" the chip I/O to an area array thereby supporting a larger number of chip connections (I/Os). Here, polymers are used in the substrate which has metal circuit traces and through holes to connect the front of the substrate (chip side) to the ball pads on the back side (printed circuit board side). These substrates could be either thick film based with conventional through hole plating and thick Cu paste as conductors or thin film based which used sequential build-up processes based on thin polymer dielectrics (35-40 μm film thickness). These packages use a solder reflow process to interconnect the package substrate to the PCB which required the use of photo-imageable epoxy-based polymers as solder masks. The next revolution created the flip-chip ball grid array (FCBGA) type packages where instead of using a wire-bond, solder balls are attached to the active side of the chip and the chip is mounted on the substrate using a reflow process to make metallurgical interconnections. This led to the use of underfills to stabilize the solder joints and counter failure because of co-efficient-of-thermal-expansion (CTE) mismatch between the chip (3-4 ppm/^{o}C) and the substrate (17-20 ppm/^{o}C).

Underfills are polymeric materials with controlled viscosity and CTE. Thus, we can see that polymers have been critical to several aspects of the package substrate.

Driven by movements towards further miniaturization and higher functionality, advanced packaging platforms require advanced materials to achieve better performance. The common characteristic of all emerging applications in artificial intelligence (AI), data center networking, autonomous driving, and neuromorphic computing is the requirement of high-speed, low-power interconnects. Different advanced packaging platforms such as wafer-level packaging or panel-level-packaging (PLP) are currently being investigated to enable these applications, and polymeric materials with excellent electrical, physical, mechanical and chemical properties offer an attractive solution for meeting these needs and the market revenue for these polymeric materials is poised to double over the next 5 years [2]. The maximum revenue is expected to come from the dielectric materials market which is used for the RDL layers in these advanced packages. The important performance metrics that are influenced by the choice of the dielectric material is the signaling speed and wiring density. Figure 2 summarizes the trend in polymer dielectrics as used in RDL wiring layers and highlights the need for low-D_k polymers. Co-fired ceramics based LTCC (low-temperature co-fired ceramic) and HTCC (high-temperature co-fired ceramic) packages have thick metal-oxides as the dielectric material with a D_k>8.0. Silicon back-end-of-line (BEOL) based RDL uses ultra-thin SiO_2 with a D_k of ~4.0. Advanced organic laminated use epoxy-based polymer dielectrics with a D_k of >3.0 and dielectric thickness of >20 μm. The focus of this dissertation is to extend advanced polymer dielectrics by overcoming the challenges associated with moving to ultra-thin, ultra-low D_k polymer dielectric materials, This thesis focuses on developing polymer dielectrics materials, processes and reliability to achieve ultra-high signal speeds while extending current wiring density to meet the requirements of ultra-high bandwidth.

1.2 Research Objectives

The specific objectives of the proposed research are:

- Develop ultra-low D_k (< 3.0) and ultra-thin polymer dielectric materials with optimal properties for high-signal speed
- Develop panel-scale processes for ultra-thin dielectrics with high surface planarity capable of supporting fine line/spaces of < 2 μm line width/space and < 5 μm diameter vias
- Investigate the thermo-mechanical and chemical reliability of polymer/copper interfaces

The detailed objectives of this thesis work with the target values are given in Table 1. The primary goal is to develop the next generation polymer dielectric materials by tackling the fundamental challenges of moving towards ultra-low D_k and ultra-thin dielectric materials which are panel-scalable and have reliable interfaces. A schematic of the proposed contributions to specific challenges in polymer RDL is shown in Figure 3. As the first objective to develop ultra-low-D_k and ultra-thin dielectric materials with the right properties, this research will demonstrate the performance benefits in using ultra-low-D_k dielectrics and present a materials selection criterion. Currently used polymer dielectric materials classes will be compared in terms of a broad range of material properties and other parameters to select upfront the appropriate materials class. This work will demonstrate to materials suppliers the need to develop ultra- low-D_k, ultra-thin dielectric materials to enable emerging applications. This work also helps identify the exact application space for these low-D_k materials and understand the fundamental trade-offs in materials selection for RDL. For the second objective, to develop panel-scale processes for ultra-thin dielectrics with high surface planarity capable of supporting fine line/spaces of < 2 μm line width/space and < 5 μm diameter vias, this thesis will demonstrate the process conditions required to achieve smooth

planar surfaces with dry-film and liquid polymer dielectrics. Further, the benefits and challenges using advanced fly-cut planarization processes will be discussed. For the third objective to investigate the thermo-mechanical and chemical reliability of polymer/copper interfaces, this work will looks into a) evaluating the effect of polymer co-efficient of thermal expansion (CTE) and young's modulus (Y) on the RDL reliability, and b) exploring techniques to improve polymer/copper interfacial adhesion with ultra-low D_k dielectrics.

Table 1 Research objectives

		Parameters	**Target**	**Prior Art**
Ultra-low D_k polymer dielectrics	Electrical	D_k	< 3.0 (1 MHz-GHz)	>3.0
		D_f	< 0.001	> 0.014
	Mechanical	Elongation to failure	>30%	2.5– 45%
	Chemical	Moisture absorption	< 0.2 wt. %	0.2 – 1.5 wt.%
Ultra-thin polymer dielectric processes	Planarity		>80% with panel-scalable processes	> 80% with non panel-scalable processes
	Dielectric thickness		1-2 µm	>25 µm
ULK and UT polymer dielectric reliability	Thermo-mechanical Reliability	• Residual Stress, and • Strain	• < 90MPa • <0.012	-
	Chemical Reliability	Adhesion	>0.3 kgf/cm	0.2-1 kgf/cm

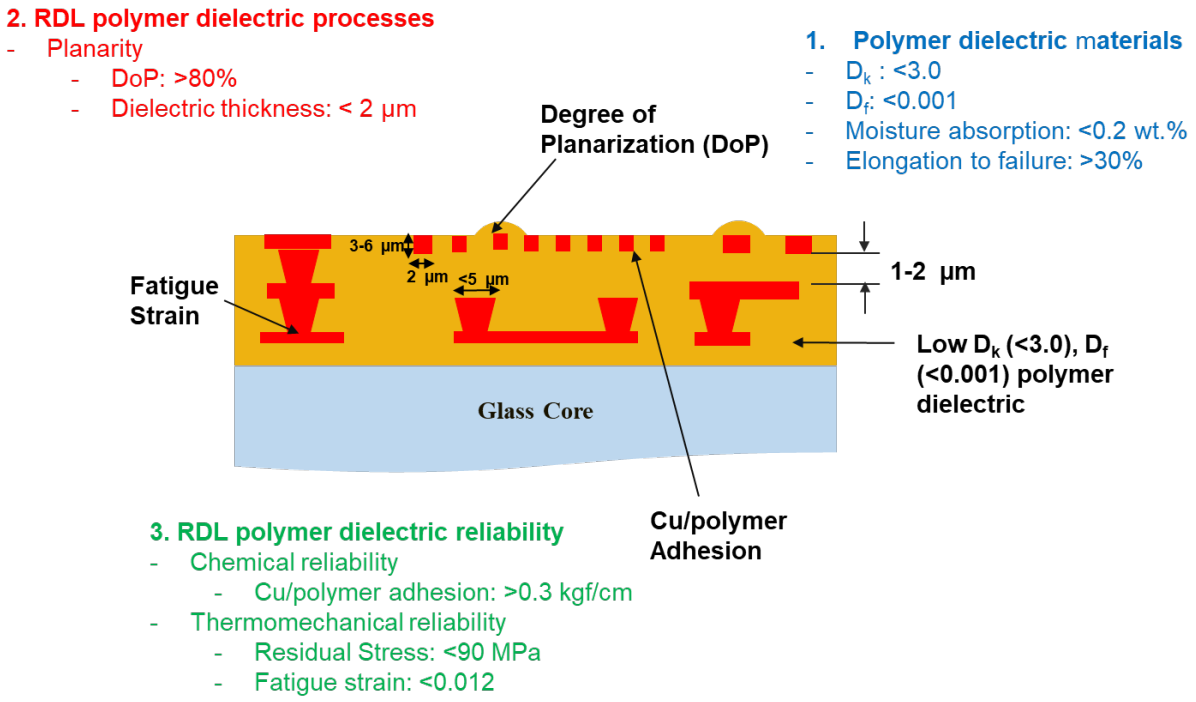


Figure 3 Proposed ultra-low D_k and ultra-thin polymer dielectric materials, processes and interfacial reliability for ultra-high bandwidth

1.3 Technical challenges and research tasks to address them

The technical challenges associated with the objective and the research tasks to address them are given in Table 2. The first task is to perform an upfront selection of ultra-low D_k materials depending on polymer structure and property and characterize performance improvement with low D_k materials for high-speed signaling. The challenge here is that current dielectrics cannot support the data rates needed for ultra-high bandwidth. This task evaluates different polymer dielectric material classes to identify advanced dielectric materials of interest based on the thesis objectives. Further, electrical design, fabrication and characterization will be performed to demonstrate the bandwidth increase with ultra-low D_k, ultra-thin dielectrics.

Table 2 Technical challenges and research tasks to address them.

	Technical Challenges	Research Tasks
Ultra-low D_k polymer dielectric materials	1. Current dielectrics do not meet the ultra-low D_k target and cannot support data-rates needed for next-generation ultra-high bandwidth	1. Ultra-low D_k materials selection depending on polymer structure and property and characterize performance improvement with low D_k materials for high-speed signaling
Ultra-thin polymer dielectric processes	2. Current processes cannot support high RDL density across panel-scale with ultra-thin dielectrics	2. Develop panel-scalable ultra-high density RDL processes for ultra-thin, ultra-low D_k dielectrics with least DoP
Thermo-mechanical reliability of ULK and UT polymer RDL	3a. Ultra-thin, ultra-low D_k dielectrics increases RDL stress and interfacial strains	3a. Investigate effect of dielectric material properties on RDL reliability
Chemical reliability of ULK and UT polymer RDL	3b. Ultra-low D_k materials are non polar and have poor adhesion to copper	3b. Investigate surface modification techniques to improve adhesion

The second task is of developing panel-scalable ultra-high density RDL processes for ultra-thin, ultra-low D_k dielectrics with least DoP. The challenge here is that currently no processes exist for deposition of ultra-thin dielectrics to create high RDL density. This task develops optimal deposition processes for <5 μm dielectric thickness for both dry-film and liquid dielectrics using panel-scalable processes. The third task, is of creating reliable polymer/metal interfaces. The key challenges here are a) ultra-thin, ultra-low D_k dielectrics increases the interfacial strains and RDL stress b) ultra-low D_k dielectrics are non-polar and have poor adhesion to copper. To tackle the first challenge, the effect of polymer dielectric material properties on RDL reliability is investigated. This involves simulation and experimental validation to develop a predictive model for copper/polymer interfacial strains in < 5 μm diameter copper microvias. To tackle the second challenge, a surface modification technique is developed for increasing polymer/copper interfacial adhesion. This involves exploring a novel technique of vapor-phase-infiltration (VPI) to modify the sub-surface of the polymer.

1.4 Thesis Outline

Chapter 1 defines the strategic need for this work, identifies research objectives to go beyond prior art, discusses the technical challenges in achieving the research objectives and defines research tasks to address these challenges

Chapter 2 describes the prior art and identifies the gap between the existing solutions and the need for next-generation high-performance RDL dielectric materials.

Chapter 3 focuses on materials structure and property correlation and selects material classes of interest from fundamental properties. The maximum signaling data rates for ultra-low D_k, ultra-thin polymer dielectrics will be studied and characterized. Design and demonstration of fine-pitch (< 5 μm) single and coupled microstrip transmission lines for selected material classes will be described. The insulation resistance for the material candidates of interest will be presented before and after a moisture stress test.

Chapter 4 describes the processing techniques to deposit ultra-thin dielectric films over a non-planar substrate. It focuses on developing a process for fabrication and characterizing the surface planarity for ultra-fine pitch (<2 μm line space/width) wiring using ultra-thin, ultra-low D_k dielectrics. The work presented will extend the limits of current advanced packaging RDL formation processes and study the fundamental limitations associated with scaling to ultra-thin dielectrics.

Chapter 5 identifies the reliability challenges associated with ultra-fine-pitch high-density RDL using ultra-thin, ultra-low D_k dielectrics. Specifically, the thermo-mechanical and chemical reliability of the polymer/copper interface will be discussed. A finite-element-modeling approach will be presented to predict the strains at the copper/polymer interface and this model is validated with experimental study. A

novel vapor-phase-infiltration approach will be discussed to increase interfacial adhesion between the copper and ultra-low D_k polymer.

Chapter 6 summarizes this scientific and technical contributions from this work and describes points of extension for future work.

CHAPTER 2. LITERATURE REVIEW

Dielectric materials are used as insulators between the copper wiring to achieve isolation and drive high-speed signals. In this chapter, a critical review of the relevant prior work with ultra-low D_k, ultra-thin materials, processes and reliability will be discussed. The dielectrics used in advanced packaging and the material selection criteria for these packages will be highlighted in the first section on dielectric materials. The important structure-property-process-performance relationships between dielectric materials will be discussed and the gaps in literature will be identified, the second section discusses the deposition process for these materials and the techniques to coat a planar surface. This section will also highlight the processing techniques used in advanced re-distribution layer (RDL) wiring and discuss the advantages and limitations of each process. The third section details the interfacial reliability of ultra-low D_k, ultra-thin dielectrics. Critical polymer/copper interfacial strains and their effect on thermo-mechanical reliability of the RDL is discussed in the first part, followed by strategies to increase the polymer/metal interfacial adhesion.

2.1 Dielectric materials:

Heterogeneous integration comprises of using packaging to integrate dissimilar chips with different functions from a variety of manufacturing sites into a system. These dissimilar chips talk to each other with via the re-distribution layer (RDL). The material of choice used in the RDL plays an important role in determining the number of interconnections between the chips, which makes it critical to determine the line/space supported by the material and the process flow to enable it. Advanced packaging architectures aim to bring chips closer together and enable faster access to data with low latencies. Table 3 compares different advanced packaging architectures on the basis of the dielectric material used in RDL,

the minimum line/space routing demonstrated, the fabrication process flow and the packaging architecture used. It is a representative list of the material classes used in current advanced packaging architectures.

Table 3 Comparison of Polymer Dielectric materials in high performance packages

	Material	**D_k**	**RDL, Line/Space** **Via diameter**	**Thickness of dielectric**	**Process**	**Type of Package**
Shinko's Organic Interposer (i-THOP)	Photosensitive-resin	3.0-3.5	2/2 μm (R&D) 10 μm	>3 - 10 μm	SAP	Interposer (Panel)
Amkor (SWIFT)	Polyimide (PI)	3.0-3.6	2/2 μm (R&D) 10 μm	>15 μm	SAP	Fan-Out (Wafer)
SEMCO	Polybenzoxazole (PBO)	3.1	2/2 μm (R&D) 6 μm	>5 μm	RDL First	Fan-Out (Panel)
Amkor (SLIM)	Silicon oxide	4	<2/2 μm (R&D) -	>2 μm	BEOL	Interposer (Wafer)
Intel EMIB	Silicon oxide	4	2/2 μm (Product) -	>2 μm	BEOL	Fan-Out (Panel)
Xilinx	Silicon oxide	3	<0.5 μm (Product) -	>2 μm	BEOL	Interposer (Wafer)

Cisco	-	-	6/6 µm (Product)	-	SAP	Interposer (Panel)
Kyocera APX	-	>3.0	6/6 µm (R&D) >10 µm	>8 µm	SAP	Interposer (Panel)
Glass Interposer	Ultra-low D_k dielectric	<3.0	2/2 µm (R&D) 3 µm	<3 µm	SAP	Panel

2.1.1 Polymer dielectrics

This section describes the polymer dielectric materials used current advanced packaging architectures.

2.1.1.1 Shinko's ITHOP with photo-sensitive resin

Shinko's thin-film RDL on build-up package substrate test vehicle is shown in Figure 4 and uses a photo-sensitive resin as the fine-pitch fabrication layer [3]. It is meant for high-performance applications and is a 4+(2-2-3) test vehicle, that consists of a 2-layer metal core, three build-up layers on the PCB side, two build-up layers on the chip side and 4 thin-film copper wiring layers on the surface of the RDL layer. The thin-film wiring layers have a minimum feature size of 2 µm lines and they are interconnected with a 10 µm via to the bottom layers. The coarse build-up layers are made using semi-additive processes and the topside is finished with a chemical-mechanical-polishing (CMP) step to smoothen the surface for the final fine-pitch wiring. A thin-film process is used for the high-density layers with spin-on photoresists, exposed using a stepper tool and a Ti/Cu seed layer for metallization. Although this was a first demonstration of fine-pitch wiring on an organic interposer it suffers from RDL yield issues.

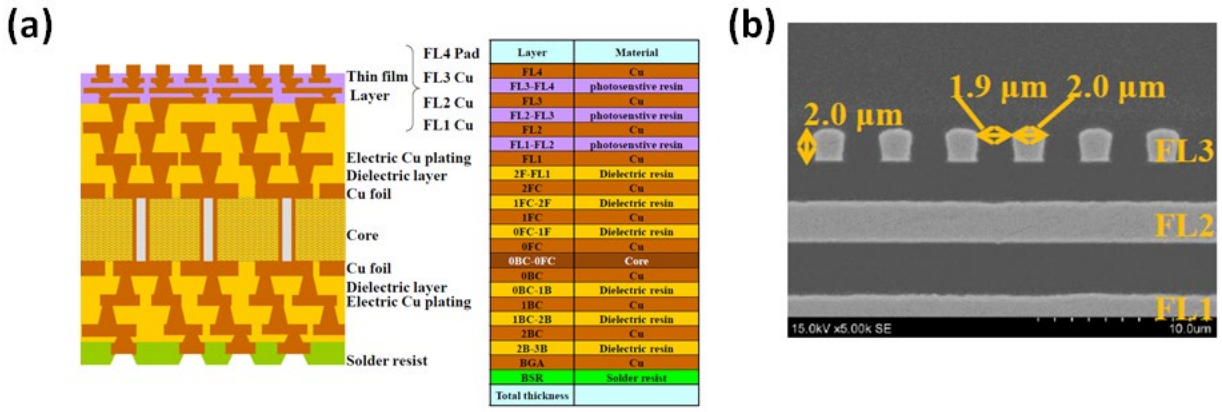
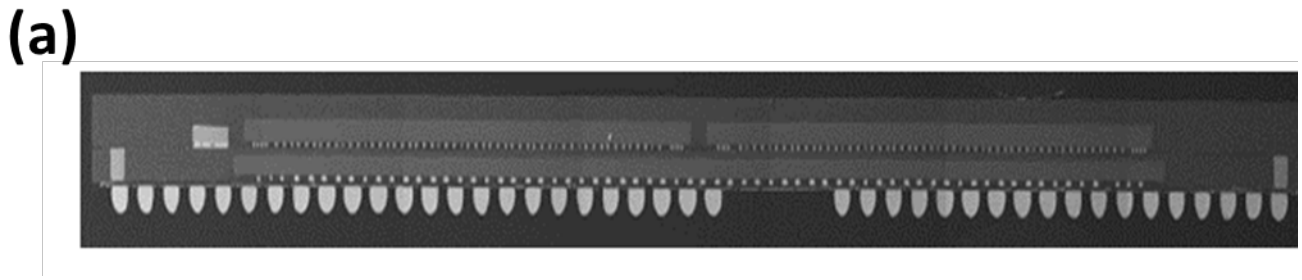


Figure 4 (a) Cross-section schematic of organic interposer (iThop) (b) 2 µm line/space on fine line

2.1.1.2 Amkor SWIFT with polyimide

The SWIFT test vehicle consists of a PoP (Package on Package) type structure and uses a chip-last process. The multi-layer RDL is built on a carrier wafer onto which the chips are assembled, and tall Cu pillars are made to bond to the bottom die which is overmolded. The minimum line thickness in the multi-layer RDL is 2 µm and the dielectric used is polyimide [4, 5], and it is spin-coated on the wafer. Although this architecture enables shorter interconnection length because of multi-die stacking, it faces significant thermal challenges and is suitable for the mobile application process or mid-range high-performance computing applications which require less power.



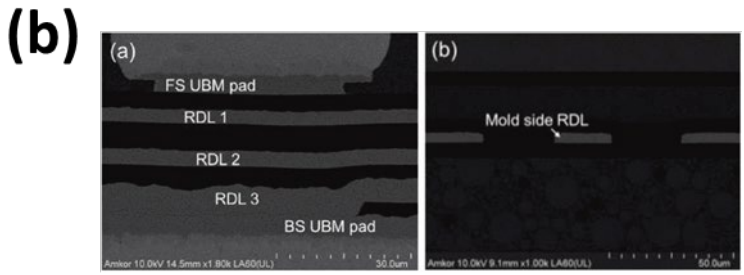


Figure 5 (a) Cross-section schematic of 3D SWIFT from Amkor with one IC die (11 mm) at the bottom and two IC dies (6 mm X 10mm) on the top layer (b) RDL cross-section on the multi-layer and RDL side [4]

2.1.1.3 Samsung RDL-First Fan-Out Package with PBO

Samsung's fan-out package is fabricated using a chip-last process where the RDL is formed first on a carrier and then the die is bonded on the carrier and overmolded to create the structure shown in Figure 6 and it is capable of supporting a < 2 µm line/space RDL on the carrier. Photo-imageable dielectrics with major resin content as PBO was used as the passivation or dielectric layer [6].The key advantage of this package is that it is panel-scalable.

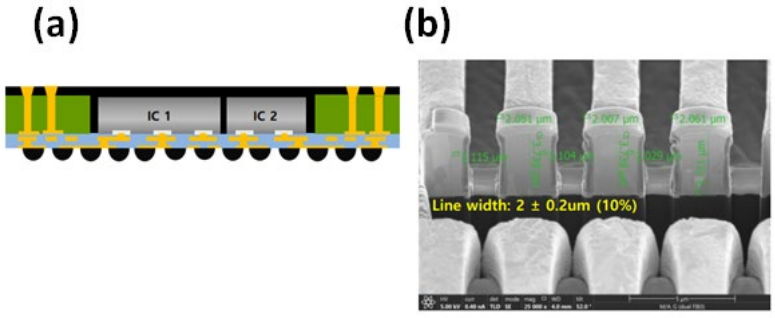


Figure 6 (a) Cross-section schematic of SEMCO's RDL-First Fan-Out Panel-Level-Package (FOPLP) (b) 2 µm line/space RDL as minimum routing feature [6]

2.1.1.4 Cisco's Organic Interposer

Cisco's organic interposer consists of a high-performance ASIC die attached on top of an organic interposer along with four HBM (high-bandwidth-memory) stacks as shown in Figure 7. The fine-pitch wiring was limited to 6 μm line/space on the top and bottom of the interposer.

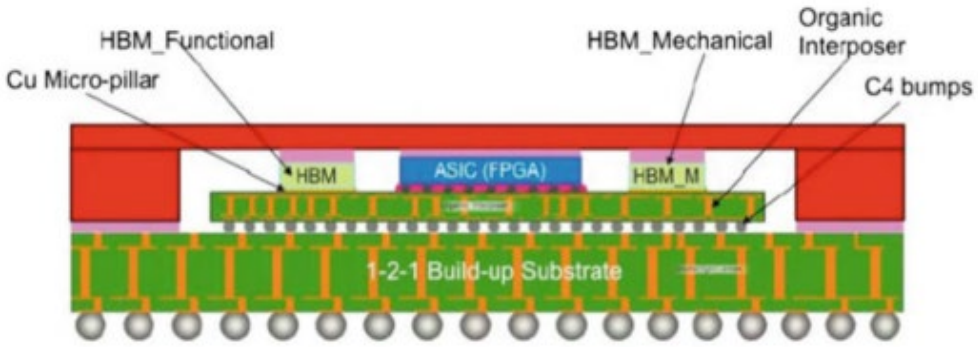


Figure 7 (a) Cross-section schematic of Cisco's organic interposer

2.1.2 Inorganic dielectrics

Silicon interposers make use of a silicon manufacturing process such as a 65 nm or 45 nm node process to interconnect multi-dies on the interposer which are then assembled on a substrate. In general, the RDL routing is not limited by feature size and can scale to submicron lengths by leveraging known wafer-level packaging processes. Figure 8 (a) shows an example of a Si interposer currently in production. Xilinx's Si interposer is used to connect multiple FPGAs (field-programmable-grid-array) with transceiver circuits and is one of the first demonstrations of heterogeneous multi-die integration [7]. This was fabricated and assembled using TSMC's 3D IC chip-on-wafer-on-substrate (CoWoS) process [8]. Other examples of Si interposers include AMD Radeon Fury device which is a fully integrated GPU-HBM package with over 22 disparate dies in a single package [9]. The Amkor SLIM is a non-TSV (through-silicon-via) based process which has both Cu and Al based RDL [10]. Figure 8 (b) shows a cross-section schematic of the architecture proposed by Intel called the embedded multi-die interconnect bridge (EMIB)

where lateral communication between chips is done using an embedded bridge with silicon-based RDL [11]. Other alternate embedded interposer type architectures have also been proposed earlier by Unimicron using a glass interposer embedded in an organic package [12], but EMIB offers an advantage of being lower cost as it uses a TSV-less process flow.

The typical process flow for inorganic RDL consists of PECVD (plasma-enhanced chemical vapor deposition) to deposit SiO_2 followed by photolithography and RIE (reactive-ion-etch) to open vias on the dielectric. RIE is also used to etch more of the dielectric and create a "dual-damascene" structure which is then metallized using a seed layer of Ti/Cu sputtered and electroplated to fully fill the trenches. Chemical-mechanical-polishing (CMP) is used to remove the excess overburden copper. The steps are repeated to fabricate additional RDL layers. The major limitation of the Silicon interposer using BEOL (back-end-of-the-line) processes is in communication applications where high-speed serial I/O connectivity is important, achieving good signal integrity is non-trivial and channel optimization has to be carefully done to achieve high-speed signaling. Other critical factors include warpage and reliability. Silicon interposers are assembled onto an organic package substrate creating CTE mismatch, as a result of which ensuring coplanarity of the bumps during assembly and controlling interlayer dielectric (ILD) stress becomes important.

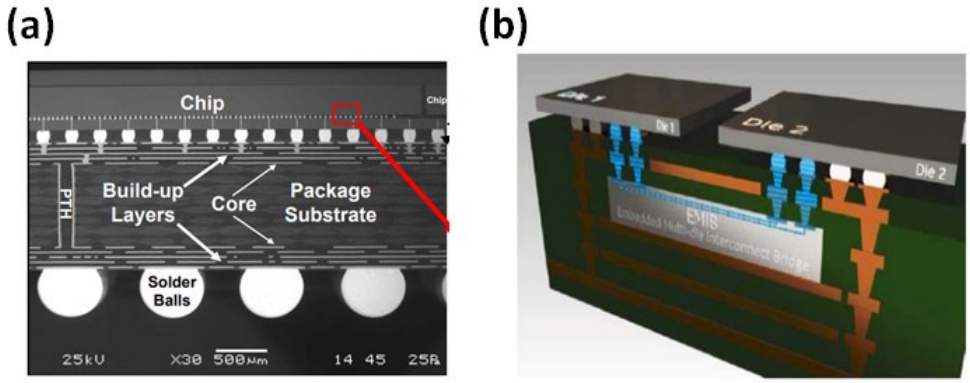


Figure 8 (a) Xilinx Silicon interposer [13], (b) Embedded multi-die Interconnect Bridge (EMIB)[11]

2.1.3 Advanced ultra-low D_k and ultra-thin dielectrics

Glass presents a unique opportunity to scale bandwidth at a lower cost because of; a) smooth surface finish and low total thickness variation which enables interconnect line width scaling down to 1-2 µm across a panel, b) low dielectric constant and loss tangent compared to silicon improves signal speed and power, c) tailorable co-efficient-of-thermal-expansion which enables direct board attach and eliminates the package substrate [14, 15].

Although Silicon interposers with back-end-of-the-line (BEOL) can handle sub-micron RDL with 1-2 µm line/spaces, they are limited by high electrical resistance due to ultra-thin copper conductor traces and high capacitance because of SiO_2. Organic interposers are capable of panel-scaling but are limited due to thick dielectrics driven by poor dimensional stability of the cores which does not support fine line/spaces. Glass interposers which use glass as the core material offer a compelling alternative by being panel-scalable and able to support fine line/spaces at potentially lower cost.

Organic-RDL that are based on low-D_k polymers offer a compelling alternative as they can meet the I/O density requirement, while also reducing the resistance and capacitance of the interconnects, thereby allowing for higher data rates.

For high-performance digital applications when the interconnect length becomes comparable to the wavelength, transmission line (TL) effects become prominent. The signaling rate of silicon interposers is limited to 6 Gb/s with a 50 ps rise time for 6 mm long links between HBM and Logic dies [16]. A differential voltage of 50 mV is considered reasonable for cross talk but is flexible based on the interposer design. A feasibility study on fine lines using organic polymer dielectrics indicated that for a dielectric constant of 3.0 there can be a 1.3X improvement in bandwidth at 20 GHz. The dip in the bandwidth seen at the transition from 2 to 1 μm trace width indicates the high resistive losses because of the increase in surface roughness of the copper traces being comparable to the trace width and is shown in Figure 9 (b) [17]. For inorganic dielectrics, several design optimizations and characterization studies have been carried out for the 2.5D silicon interposer to propose the most efficient routing interconnect structure between the high-bandwidth-memory stacks (HBM) and the logic devices [18-20]. The most optimum design was determined using both time-domain and frequency-domain simulations to study the insertion loss and eye diagrams by varying the line density based on line width and space, increasing line spacing to reduce crosstalk and increasing line width to reduce insertion loss [18].

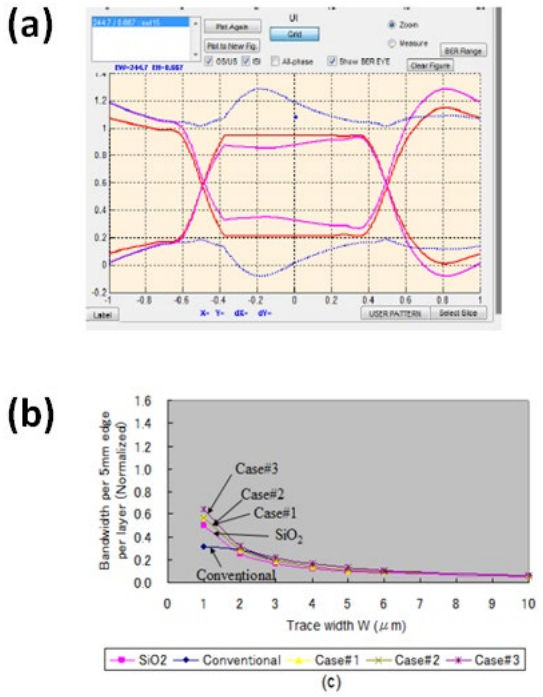


Figure 9 (a) Crosstalk reduction by equalization which increases the edge rate [16], (b) Bandwidth for different dielectrics and trace widths at 5GHz [17]

Although these studies provide theoretical validation of the limitations of the silicon interposer and the potential for scaling bandwidth based on organic RDL there still needs to be more fundamental understanding on the correlation between material property such as dielectric constant on system-level electrical performance metrics such as signaling data rates. There also needs to be input from a processing standpoint to understand what structures are feasible given the material properties. Hence, a study of the structure-property-performance relationship to characterize the performance improvements seen with changing the dielectric structure to a non-polar low-D_k type material has not been conducted and will be focused on in this thesis.

2.2 Deposition of dielectrics and fabrication of fine-pitch structures

This section details the process of depositing dielectrics and fabricating fine-pitch structures. First, the current dielectric deposition and fine-pitch fabrication processes used in advanced high-wiring density

packages are described. Second, the challenges associated with ultra-thin dielectrics with regard to depositing a uniform planar coating on non-planar RDL is described. In this section, we will look at literature from polymer processing to understand the limitations in depositing ultra-thin dielectrics on planar surfaces.

2.2.1 Dielectric processing techniques

The dielectric deposition process is dependent on the substrate process flow used. There are three different types of process flows based on the dielectric material used: polymer or organic, inorganic and hybrid process flows which are used for fabricating fine-pitch features. These processes are discussed in more detail in this section.

2.2.1.1 Processing of polymer dielectrics

Panel-scale processing of polymer dielectrics typically use vacuum lamination as the best-known-method for depositing dielectrics. However, these processes have not been demonstrated for dielectric thickness of <10 µm and ultra-fine pitch line width/space of <2/2 µm, via diameters of <5 µm. Kyocera reported line/spaces of 6 µm on an organic interposer package using 8 µm thick dielectrics which is the current state-of-the-art in production [21]. Shinko Electric Industries Co., used photosensitive dielectrics to report 2 µm fine-pitch features with a 3 µm thick dielectric in the high-density routing layer [3], however the process requires a chemical mechanical polishing step after the fabrication of the coarse-features to planarize the surface before fine-line formation. This step adds to the cost and increases the number of fabrication steps involved in the RDL formation. It was also reported that the yield of the RDL traces on panel significantly decreased when scaled to 2 µm [22]. Samsung has shown 2/2/2 µm copper line/space/height on an RDL-first process for fan-out wafer level packages, however this is currently not yet in production. The process flow as shown in Figure 10(b) shows building RDL on a bare glass carrier,

which involves spin-coating a sacrificial or debonding layer on the glass wafer followed by coating of a 10 μm thick passivation layer of a photo-imageable dielectric (PID) on a glass panel and semi-additive build-up processes to build a two-layer structure. The Figure 10 (a) shows a scanning-electron-microscope (SEM) image of the fine-features after fabrication of the first layer. It was also shown that 6 μm photo-vias with a taper of 71.3º was fabricated in the second passivation layer. Although, this is a good demonstration of the potential for 2 μm RDL, there still remain challenges to be addressed regarding the impact of surface planarity on the patterning of fine-pitch features. In this process the carrier glass used was 1.1 mm thick and a CTE (co-efficient of thermal expansion) of 8 ppm/ºC [6]. Fabrication of a second fine-pitch layer over the earlier fine-pitch layer requires low overall substrate warpage as well as high surface planarity as the available depth of focus during lithography is reduced thereby needing a shift to more expensive panel-scale stepper tools. There needs to be a more detailed evaluation of the effect of surface planarity and substrate effects on fine-line patterning.

Organic dielectrics are also used in wafer-level packages (WLP) where Polyimide (PI), Benzocyclobutene (BCB) and polybenzoxozale (PBO) are common passivation layer materials which have a market share of over 85%. The photosensitivity of the polymers used in WLP are limited to 4 μm line/spaces. Laser ablation has been shown as an efficient way to scale to sub 4 μm via diameters in these polymers [23]. These polymers are processed as liquid dielectrics which are usually spin-coated over a 300 mm wafer and have not been optimized yet for panel-scale processes.

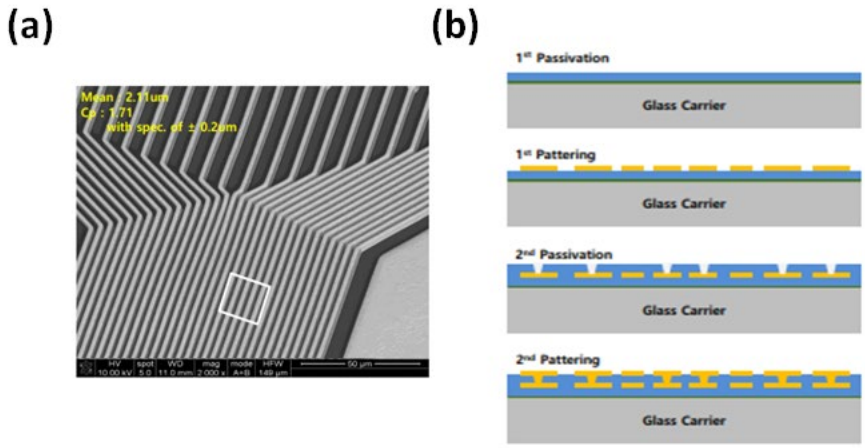


Figure 10 (a) Fine pitch features on carrier glass, (b) Process flow for an RDL-first fan-out process [6]

2.2.1.2 Processing of inorganic dielectrics

Inorganic dielectrics such as SiO_2 are used in back-end-of-line process. The line width and spacing of the RDL can be submicron and there are no limitations of scaling the feature sizes with regards to fabrication. The process flow involves PECVD (plasma-enhanced chemical vapor deposition) to form a thin layer of SiO_2 on a bare silicon wafer. Photoresist is spin-coated onto the wafer and a stepper tool is used to open the resist and reactive ion etch (RIE) is done to remove the SiO_2 selectively patterned. The resist is stripped, and a seed layer of Ti/Cu is sputter deposited on the wafer. Copper is then electrochemically deposited on the wafer followed by chemical mechanical polishing (CMP) to remove the overburden Cu and the seed layer of Ti/Cu. The processes are repeated to create additional RDL layers. When the RDL interconnect structures are formed such that the line/trench is fabricated directly over the via then it is called a dual-damascene interconnect.

2.2.1.3 Tandem processing of organic and inorganic dielectrics

To scale down to ultra-fine pitch features of < 2 µm line/spaces as shown in Figure 11 (a) a hybrid RDL approach is used which uses both organic and inorganic dielectrics. The first RDL layer is formed using BEOL process where PECVD is used to deposit the SiO_2 dielectric layer and a dual-damascene type process is used for the conductor layer. The remaining RDL layers are fabricated using an organic polymer as the dielectric that is deposited using spin-coating as shown in Figure 11 (b). The advantages of this process are that it can be used to pattern high-density layers using BEOL processes but still utilize organic RDL where it may be possible to reduce cost.

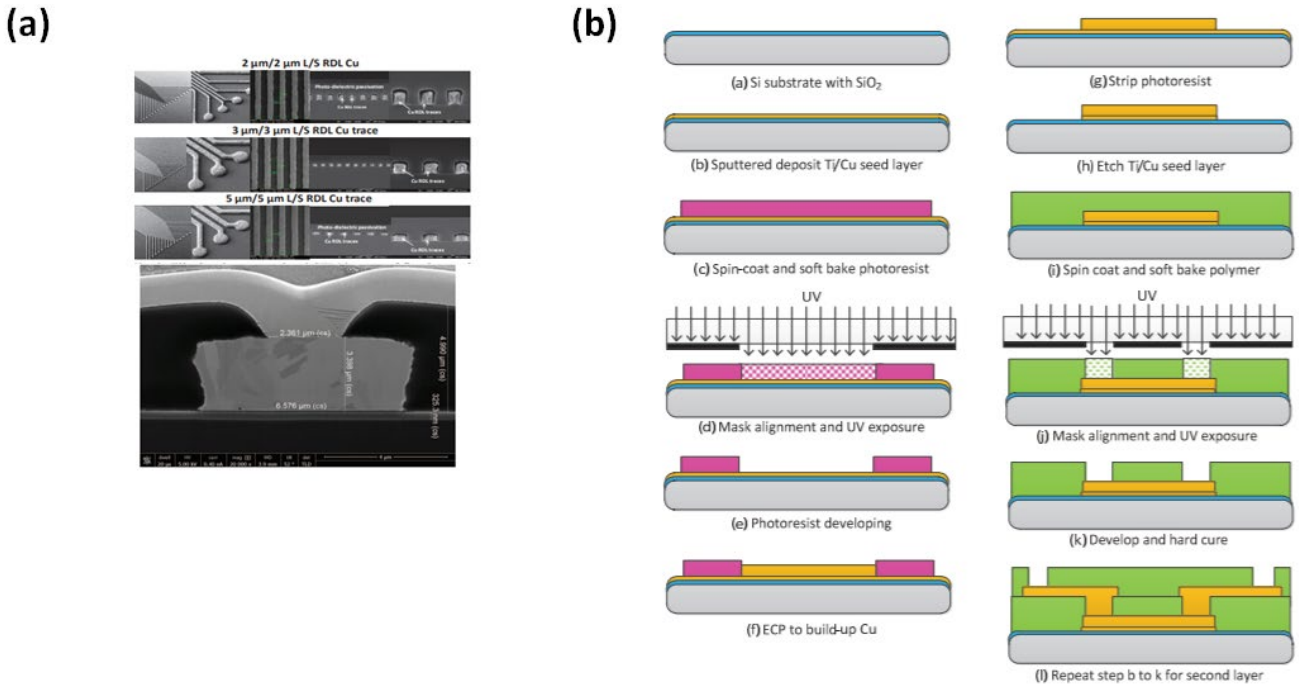


Figure 11 (a) Demonstration of 2-5 µm RDL on silicon substrate, (b) Process flow for hybrid RDL [24]

Although there are various methods of patterning below 2 µm, significant limitations of BEOL or WLP that include the planarity of the surface when using spin-coated dielectrics as well as the requirement of CMP. Further, the seed-layer etch is a critical challenge when scaling to sub 2 µm RDL as the profile

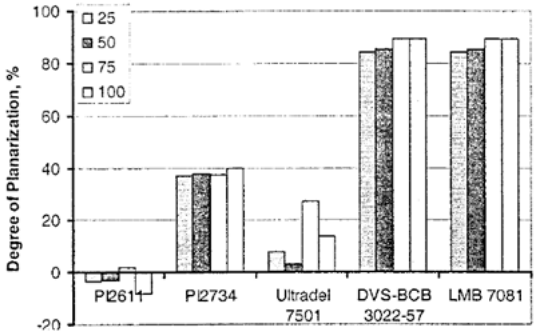
of the copper line changes and there is potential of the dry-film photo-resist falling off the surface of the seed-layer after development [25].

2.2.2 Planarity of ultra-thin polymer dielectrics

In this section, the approaches used in literature to create a smooth planar surface using polymer dielectrics are discussed. Fabrication of microstructures on multiple layers requires each layer to be planar before the photoresist is coated and imaged. The thickness variations across the panel or wafer makes it difficult to planarize the surface. Additional steps such as fly-cut planarization or chemical-mechanical-polishing (CMP) have to be used to smoothen the surface to pattern fine-line/pitch layers. Further, the viscosity of the polymer and coating parameters often determine if the film will "tent" or completely fill the gap between the copper traces. Several process variations have to be carried out to press the material using an optically flat surface to coat between fine-pitch traces. The most recent study involving planarization of polymer dielectrics was done by Chiniwalla, et al. [26], where they looked at five polymer dielectrics (including polyimides, epoxy and BCB) in single and multilayer structures with different line spacings and width. Here, two layers of the polymer coating is considered to be a multi-layer structure and the metal lines fabricated on a polymer coating and without as different test-structures, a comparison of the surface planarity observed is reported in Figure 12. These polymers were spin-coated on the test-wafer and the degree of planarization was measured using a profilometer. The test-structures investigated varied from 25-100 μm feature sizes and a 1:1 and 1:2 line width/spacing was fabricated. The key observations that can be noted from this study include, a) film shrinkage manifests itself directly as a change in thickness of the dielectric, and polyimides cure as much as 50% on solvent loss, b) flow of the polymer over the metal is related to the structure of the polymer and c) as the spacing between lines increase the DoP decreases for all polymers. Other theoretical approaches towards surface planarization in BEOL processes have looked at modeling conformal deposition of the dielectric and step coverage

based on different process parameters [27]. The effect of varying deposition conditions of the dielectric and capping layer on the coverage of the copper traces was also studied in the paper. Further work has been done to planarize the polymer film and thereby reduce dimples seen in vias but it was noticed that pressing with an optically flat surface only helps in local planarization for test-structures with vias [28].

(a)



(b)

Polymer	Feature Size	DOP1	DOP2	DOP2 (predicted)
PI 2611	25	-3.49%	8.69%	-7.09%
	50	-3.27%	9.92%	-6.64%
	75	2.04%	38.64%	4.03%
	100	-8.33%	8.23%	-17.35%
PI 2734	25	37.00%	61.93%	60.31%
	50	37.68%	61.79%	61.16%
	75	37.36%	63.26%	60.76%
	100	39.97%	62.81%	63.96%
Ultradel 7501	25	7.78%	7.87%	14.96%
	50	3.27%	8.51%	6.44%
	75	27.30%	68.72%	47.15%
	100	13.81%	26.09%	25.71%
DVS-BCB 3022-57	25	84.33%	97.65%	97.54%
	50	85.37%	97.79%	97.86%
	75	89.33%	94.98%	98.86%
	100	89.34%	95.83%	98.86%
LMB 7081	25	76.25%	79.35%	94.36%
	50	75.17%	76.38%	93.83%
	75	89.51%	84.42%	98.90%
	100	87.84%	82.44%	98.52%

Figure 12 (a) Single layer planarization for features with 1:1 line/width spacing, (b) Degree of planarization after 1) one layer of polymer (DoP1) 2) two layers of polymer (DoP2) [26]

A study by Fruanhofer IZM done on wafer-level-packages (WLP) looked at different spin-coated polymers and calculated the DoP of these polymers at a Cu height of 5 µm, dielectric height of 9-10 µm. BCB polymer performed significantly better compared to other polymers as shown in Figure 13[29].

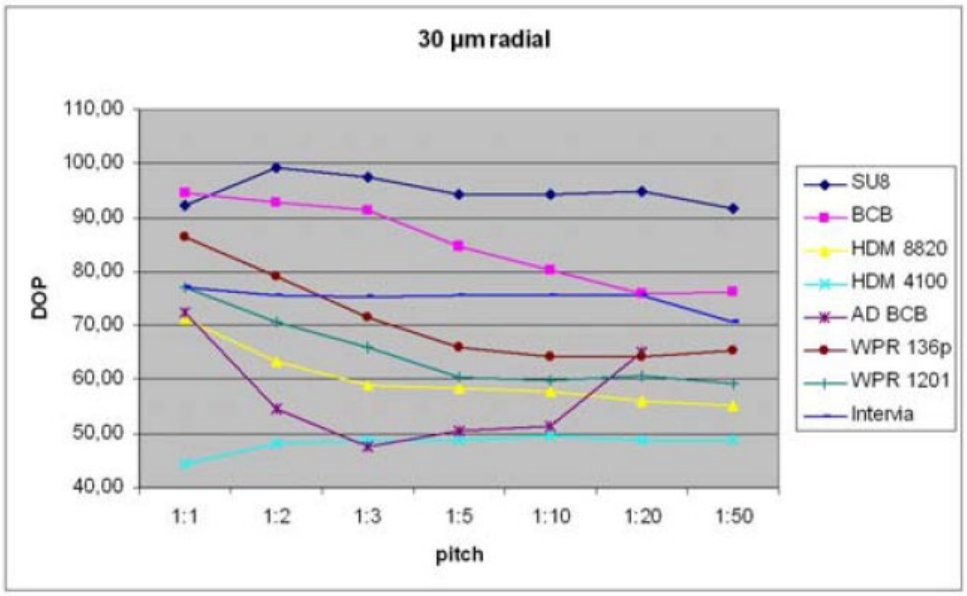


Figure 13 DoP for 30 µm line width with varying line spaces [29]

Although the wafer studies are useful to understand the parameters to test for surface planarity of RDL, there has not been a complete quantification or even methodology established to evaluate and characterize the surface planarity of fine-pitch multi-layer polymer RDL. It is important to understand the limit of patterning sub-2 µm traces on a non-flat surface and this thesis will explore this area.

2.3 Reliability

In this section, the thermo-mechanical and chemical reliability of the polymer/copper interface is discussed.

2.3.1 Thermo-mechanical reliability

Mechanical failure in packages originates as a result of fatigue failure due to residual strains from thermal processing. In this section, the strains associated with two types of interconnect structures are discussed.

2.3.1.1 Vertical interconnects

Vertical interconnects or microvias are of great interest because they can enable higher interconnect density over multiple layers. Microvias have evolved from 150 µm diameter in organic laminate packages to < 5 µm in advanced packaging architectures. These microvias can either be stacked or staggered to enable connected between multiple levels. The reliability of microvias has always been of concern since they were first introduced [30]. The most common methodology to assess the reliability of microvias is either thermal shock or thermal cycling which takes the package to extreme temperatures (125 ºC to -55 ºC or -40 ºC) and aggravates the co-efficient of thermal expansion (CTE) mismatch at the polymer/metal interface. This manifests as via cracking at the microvia/pad interface as shown in Figure 14. There have been efforts to build a predictive model for microvia reliability however these are for > 150 µm diameter as shown in Figure 15. Further there has also been experimental work and modelling work for > 25 µm diameter vias which study the effect of geometry and material properties on the fatigue strain [31]. Similar methodologies are used to study the reliability of < 5 µm diameter vias in this thesis and understand the impact of material properties on the residual stress.

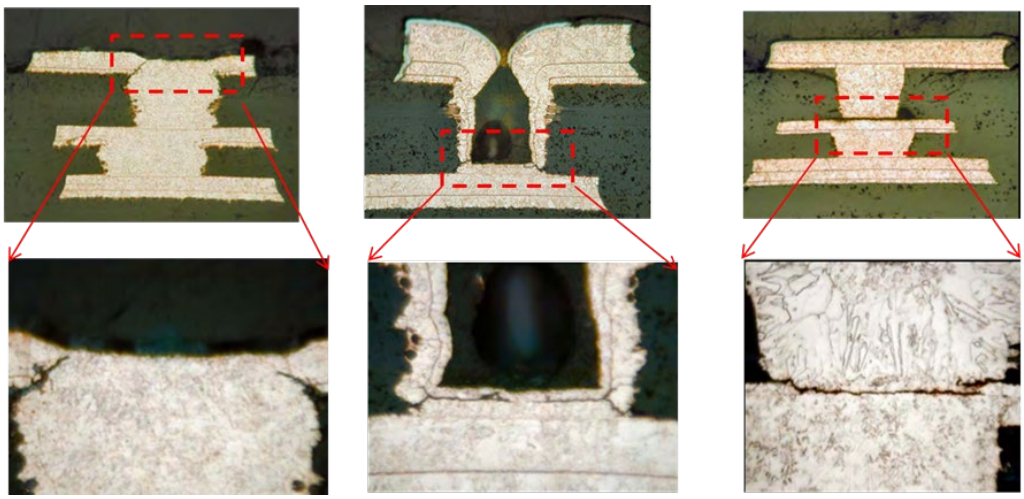


Figure 14 Via cracking after TCT because of CTE mismatch [32]

Table 10: First-Order Model with No Interactions

	Estimate	Std. Error	t value	Pr(>|t|)
(Intercept)	-2.30E-03	1.31E-03	-1.75	0.0886
T	5.11E-05	1.16E-05	4.403	9.17E-05
D	-3.87E-05	5.81E-06	-6.67	8.94E-08
A	1.09E-04	1.66E-05	6.548	1.29E-07
E	1.71E-04	7.26E-05	2.354	0.0242

Figure 15 Regression model for stacked microvia reliability (> 150 µm diameter) [33]

2.3.1.2 Lateral Interconnects

Thin-film deposition processes often induce stresses on the substrate and compressive residual stresses cause film buckling and debonding. This film buckling provides a pathway for moisture propagation and can lead to loss of film adhesion. Other sources of stress are the bending stress because of substrate warpage. The main material properties which influence the residual stress are the young's modulus and CTE of the polymer. To qualify the dielectric materials for long-term reliability standards, other properties such as ultimate tensile strength, elongation at break and substrate warpage come into play. There was a study on the residual stress within polymer layers as a key parameter for system-level

reliability [34]. The origin of stress was found to be dependent on the curing profile of the polymer and polymer tailoring was conducted based on different formulations of polyimide to reduce the stress as is shown in Figure 16 (a) . Compared to the stress measurements on polymer dielectric films, thin-film stresses in metal films have been well studied and understood. The deposition temperatures of sputtering, evaporation, electroplating or chemical vapor deposition (CVD) often influence the grain structure and size which determine the film stress. It is also known that as the temperature of deposition increases, recrystallization and grain growth occur and the stress changes from tensile to compressive stresses for metal thin films [35].

The residual stress in a thin-film can be divided into the intrinsic stress and the thermal stress [36]. When the stress in a film is compressive as expected for polymer RDL layers, there are two dominant failure modes namely, a) buckling driven interface delamination, and b) edge delamination. The most common failure mode in PCB substrates which comprise of multiple organic RDL layers is buckling driven delamination as shown in Figure 16 (b). And there have been simple equations which correlate the compressive stress to the required peel strength of the interface as given by equation 2 [37].

$$\sigma_{critical} = PS/d_{cu} \quad (2)$$

Where, $\sigma_{critical}$ is the critical compressive strength, PS is the required peel strength and d_{cu} is the thickness of the copper film. However, this applies only for a blanket copper film over a substrate and does not take into account plasticity effects and is based on Elastic Plastic Fracture Mechanics (EPFM) [38]. There's also potential of interfacial delamination in polymer thin-film RDLs and the adhesion strength required for that is tested using peel strengths. Usually in thin film delamination, a large plastic zone often forms around the fracture region which dissipates most of the applied energy and the large

plastic effects can disrupt the stress distribution around the peel area, which makes applying traditional EPFM based equations to characterize the stress not acceptable.

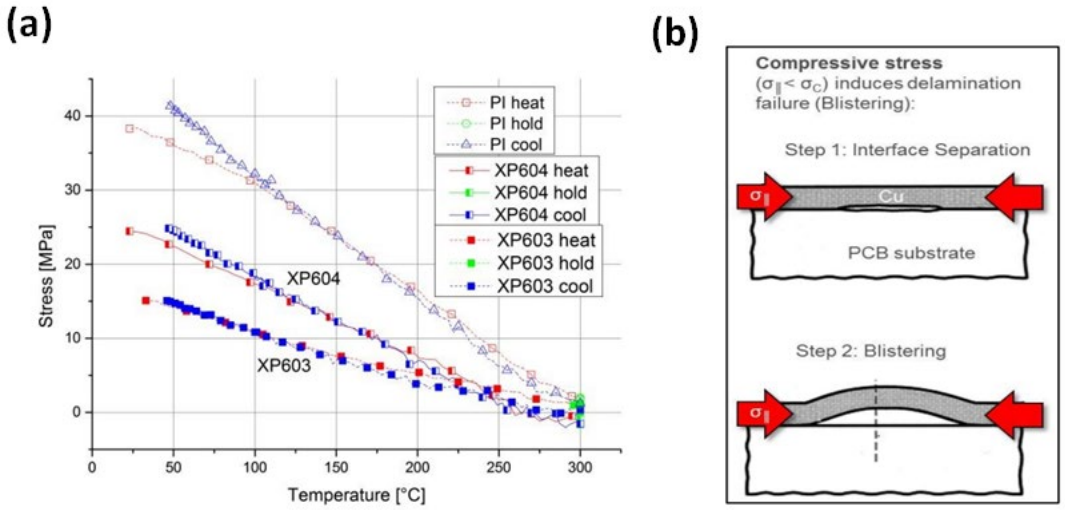


Figure 16 (a) Residual stress with different formulations of PI [34], (b) Compressive stresses inducing delamination [37]

Based on the above discussion, clearly there is a need to characterize the residual stress as a function of the polymer structure along with the deposition processes used. This will provide insight to better design polymer systems and depositions processes to ensure that the residual stress of the polymer RDL is controlled and system-reliability standards are met.

2.3.2 Chemical reliability

Typically, low-D_k polymers are non-polar and have poor adhesion to metals and cannot be easily metallized. The non-polar groups cannot be modified because they are critical to ensuring low permittivity which is essential to low signal RC delay. There have been several reported cases of adhesion loss leading to delamination creating system-level reliability challenges [39-42]. Figure 17 shows delamination at the Cu-low k RDL interface in a wafer level package (WLP) after drop impact test. A surface-insulation-

resistance (SIR) test-board biased for 6000 hours at 200 ºC showed delamination of the comb patterns from the board for different laminate materials as shown in Figure 18 [32].

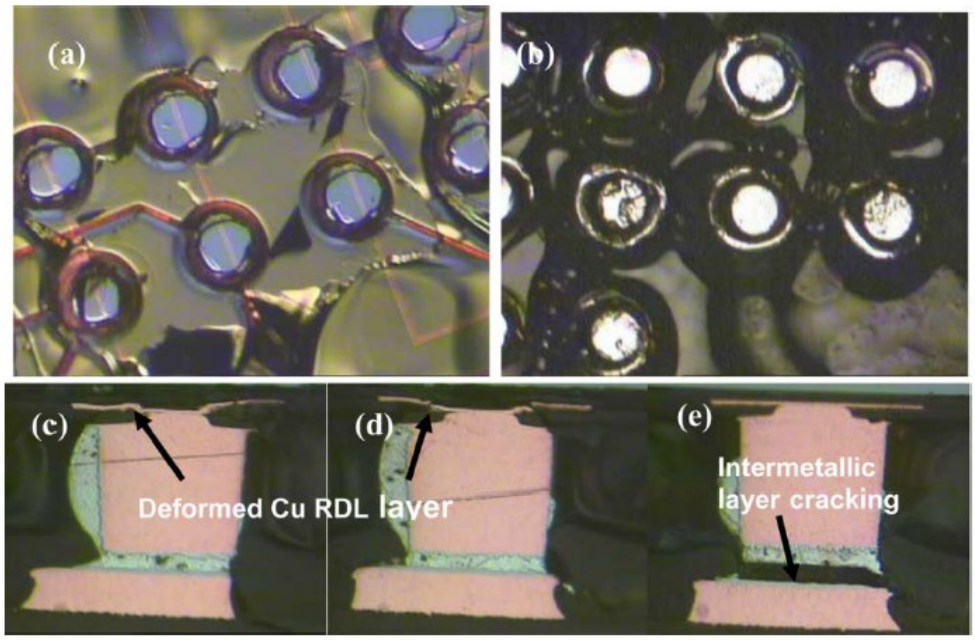


Figure 17 Adhesion induced delamination in the RDL layers on a WLP [39]

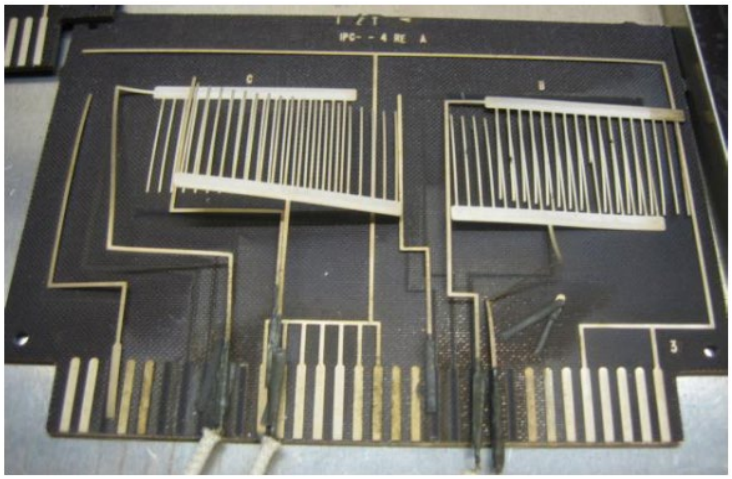


Figure 18 Delamination of copper traces from the PCB board [32]

Interfacial bonding at the metal/polymer interface is usually through, a) mechanical interlocking, and b) chemical bonding. Substrate metallization processes such as electroless copper deposition roughen the surface of the polymer to create mechanical anchors which can help in adhesion. Plasma treatment using Ar, CHF_3, CF_4 and ozone has also been used as an alternative to improve polymer/metal interfacial adhesion [43, 44]. However, these techniques induce roughness on the surface of the polymer. Currently, as we move towards <2 μm line/space it is important to maintain surface smoothness for good signal performance and for high yield in lithography. Further, as we increase the aspect ratio of Cu lines to reduce resistance, it is critical to maintain good adhesion between the copper and the polymer to ensure that the lines do not fall off.

Another area where adhesion at the polymer/metal interface is proving to be critical is in processing photo-imageable dielectrics (PID). Typically, PIDs are patterned using embedded trench based processes which involve a fly-cut planarization process similar to chemical-mechanical-polishing (CMP) on the wafer side but tailored for softer substrates. This fly-cut process is known to induce delamination and peel the metal away from the polymer as shown in Figure 19.

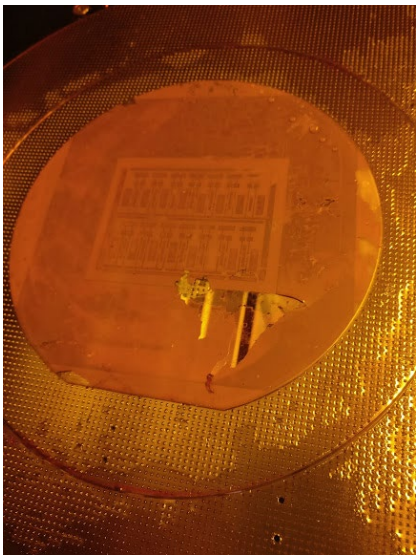


Figure 19 Fly-cut induced delamination at the polymer/metal interface

Thus, there is a need to improve polymer/metal interfacial adhesion by chemical bonding. Increasing the hydrophilicity of the polymer surface and creating a wettable weak boundary layer using adhesion promoters are employed as ways to improve the metal/polymer interface. However, intrinsic modifications have not been tried on the polymer surface and thus present a significant opportunity to improve polymer/metal interfacial adhesion.

CHAPTER 3. ULTRA- LOW D_K POLYMER DIELECTRIC MATERIALS

Ultra-low D_k, ultra-thin polymer dielectrics are critical to fine-pitch RDL for several reasons. 1) lower D_k enables potential to signal at higher data rates. 2) Ultra-thin dielectrics are needed reduce signal reflections for fine-pitch RDL by creating a good impedance match. This chapter presents a fundamental structure-property correlation for multiple dielectric material classes and identifies the key polymer groups to work with that will form the basis for the rest of this thesis. Microstrip transmission lines will be designed and characterized for fine-pitch RDL. This work will also identify the maximum signaling data rate achievable for advanced organic and inorganic RDL. Last, a brief experiment to study the insulation resistance for ultra-thin dielectrics under an aggressive test environment is discussed. This chapter is divided into two sections a) materials design and b) materials characterization.

3.1 Materials design

The polymers used in organic RDL cover a variety of material classes such as Epoxy, Polyimide (PI), Polybenzoxozole (PBO), Phenolic resins, Fluropolymers, Hydrocarbons, Benzocyclobutene (BCB) and also inorganic dielectrics which are included as metal oxides. Depending on the application as either a passivation layer material, redistribution-layer dielectric, underfill, molding compound or temporary bonding material certain material properties become more important than the other.

3.1.1 Technical approach

The choice of polymer dielectric used in re-distribution layer dielectric is driven by technology trends towards, a) high-density fine-pitch routing, b) system level thermo-mechanical reliability, and c) panel-scalable processing. Low-loss tangent and low dielectric constant are critical to maintain signal

integrity at high data-rates. Planar thin films are required for fine-pitch wiring and for impedance matching. Higher elongation to failure is favorable for multi-layer RDL with a higher copper coverage on each layer. Residual stress of the polymer is dependent on the young's modulus (Y) and co-efficient of thermal expansion (CTE). RDL fabrication processes involve processing steps such as metallization, annealing and curing which induce stresses within the polymer thin film. Further, CTE mismatch with the copper wiring and overall substrate warpage influence the amount of compressive stress seen by the polymer. There exists a critical limit of stress tolerance for fabrication of multi-layer RDL which depends on the adhesion strength of the polymer. It is essential that the material properties of the polymer are controlled to maintain the residual stress within tolerance. The moisture absorption of the polymer is critical for long-term system-reliability as often interfacial moisture absorption is responsible for delamination. Good adhesion at the polymer/metal interface is needed to fabricate multi-layer wiring structures. This adhesion is usually achieved by means of either chemical or mechanical interlocking. Recent trends toward 5G and high-frequency applications place restrictions on the copper surface roughness needed to achieve higher adhesion. This imposes restrictions on the material selection and shifts the choice towards polymers with more bonding groups that can interact with copper. The process parameters thereby narrow the selection to polymers that are compatible with existing packaging infrastructure. Table 4 compares different material classes of polymers commonly used in packaging against these criteria.

Although these properties are stated for the testing conditions, for future applications in automotive and other harsh environments, as reliability standards become more aggressive it is critical that these properties remain stable over a range of temperature, humidity and frequency.

Table 4 Comparison of polymer dielectric material families. In the color coding, green is favorable, yellow is near the target value and red indicates that the target value is not reachable.

Characteristic	Ideal Properties	Polymer Family [29]								
		Epoxy		BCB	Phenolic resin	Polyimide	Polybenz-oxozole (PBO)	Fluro-polymer	Hydro-carbon	Metal Oxide
		Non PID	PID							
Electrical	Low loss Low D_k									
Physical	Ultra-thin dry film (2-5 μm) Planar									
Thermal	Low-CTE Withstand 260 ^{0}C solder reflow									
Mechanical	High Elongation Low modulus									
Chemical	Resistance to chemicals Good adhesion									
Cost	Low Material and Processing Cost									
Reliability	Low Stress Low moisture absorption									

The properties of the polymers are compared based on commercially available as well as R&D stage polymers available and are given in Table 5

Table 5 Properties of polymer dielectric materials

	Trade Name	Electrical		Physical	Thermal	Mechanical		Chemical	Cost	Reliability
		D_k	D_f	Thickness	CTE (ppm/°C)	Elongation	Youngs Modulus	Adhesion		Moisture absorption
Epoxy	ABF T61	3.2 (5.8GHz)	0.01 (5.8GHz)	>5 µm	30 (25-150°C) 95 (>150 °C)	2.4%	7.5GPa	0.6Kgf/cm	Low	0.6 wt.% (100 °C, 1 hr)
	Taiyo PID	3.1 (1MHz)	0.017 (1MHz)	>5 µm	45	-	3.2GPa	0.5 kgf/cm	High	0.84 wt.%
Polyimide	HD 7000	3.2	0.002		50	70%	3.6GPa			1.7 wt.%
BCB	14-P005	2.57 (1MHz)	0.0008 (1MHz)	>2 µm	63	13%	2.9GPa	0.2 kgf/cm	High	0.1 wt.%
Fluropolymer	ALX 211	2.6 (1 MHz)	0.001(1 MHz)	>2 µm	60	30%	-	-		0.8 wt.%
Polybenzoxozole (PBO)	Excel CRC 8000	<2.9 (1MHz)	0.01 (1MHz)	>2 µm	55	65%	2.8GPa			<1 wt.%
Hydrocarbon	Rogers 2929	2.94 (1MHz)	0.003 (1MHz)	>50 µm	50	-	-	Low		0.1 wt.%
Metal Oxide	SiO_2	4	-	<1 µm	0.56	-	66 GPa	-	High	-
Phenolic resin	GTNO 1	2.8	0.005	~3 µm	50-60	55%	2.8 Gpa	High	High	<0.2 wt.%

Compared to other polymers, BCB has a low dielectric constant and dielectric loss, minimal moisture uptake during and after processing, very good surface planarity and a low curing temperature. 14-P005 was developed by Dow Electronic Materials based on BCB. The film thickness can be varied from (3 – 20 µm) to achieve a specific target thickness and patterning is achieved using photolithography or laser ablation. Toughening components have been added to the BCB-based film to provide the necessary flexibility while maintaining low D_k, D_f and moisture sensitivity and improving elongation and fracture toughness. Hence, BCB was chosen as one upfront material candidate for the study on low-D_k RDL polymers. The only problem was low adhesion because of the non-polar bonds in the backbone of

the polymer chain. Therefore, the other polymer dielectric material class chosen was epoxy which usually has very high adhesion to copper because of the reactive epoxide ring moiety. The other ultra-low D_k material candidate chosen was phenolic resin, however this dielectric is not currently capable of panel-scale processes. In Table 6, the properties of the specific material set used in this thesis are given. This consists of three epoxy-based materials, BCB and phenolic resin.

Table 6 Upfront material selection

		Epoxy			BCB	Phenol
		Material A	**Material B**	**Material C**	**Material D**	**Material E**
Electrical	D_k	3.2 (5.8 GHz)	3.1 (1 MHz)	3.5 (1 MHz)	2.65 (1 KHz - 1 MHz) 2.55 (1 GHz)	2.8 (10 GHz)
	D_f	0.01 (5.8 GHz)	0.017 (1 MHz)	0.022 (1 MHz)	0.0008 (1 KHz - 1 MHz) 0.002 (1 GHz)	0.005 (1 GHz)
Physical	Thickness	5 µm	5 µm	5 µm	> 1 µm	> 1 µm
Mechanical	Elongation to failure		12 - 13 %	20%	13%	55%
	CTE	30 ppm/K	40 - 45 ppm/K	45 ppm/K	45 ppm/K	50-60 ppm/K
	Young's modulus	7.5 GPa	3 – 3.5 GPa	1.64 GPa	2.9 GPa	2.8 GPa
Chemical	Curing Temperature	171 °C	180 - 185 °C	250 °C	210 - 250 °C	<200 °C
	Moisture Absorption	0.6 wt.%	0.8 wt.%	1.5 wt.%	< 0.2 wt.%	<0.2 wt.%
Processes	Resolution	<2 µm line/space	2 µm line/space	2 µm line/space	<2 µm line/space	<2 µm line/space
	Via	4 µm via (Excimer)	3 µm via (PID)	5 µm via (PID)	10 µm via	9 µm via (PID)

3.1.2 Electrical properties needed for high-speed RDL

In this study, material candidates are chosen from the previous section. These include polymer dielectrics from the epoxy, BCB and phenolic resin material families. Optimal electrical design of high-density test-structures is discussed along with preliminary results based on fundamental material

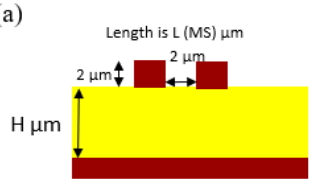
properties. Then, these test-structures are fabricated and characterized using the semi-additive process (SAP) which will be discussed in detail in Chapter 4. A model-experiment correlation will be detailed. Further, the final model based on a channel design which is representative of high-density logic-HBM interconnect signaling is built and maximum achievable data rates for the materials selected is described.

3.1.2.1 Test-structure for preliminary design

The typical-lengths of connections between logic-HBM dies are 3-6 mm [16] and the high-density wiring features are of 2 μm line/space or higher. These wiring lines are usually microstrip or stripline transmission lines, wherein the signal conductors are either above a ground plane or sandwiched between two ground planes. For the purpose of high-density interconnection layer characterization, which is typically the top two layers of a substrate it is ideal to look at microstrip lines. In this work, we looked at a surface microstrip transmission line model to study the effect of different material properties and the design rule was maintained as shown in Figure 20 (a). Si BEOL processes were taken as the baseline to benchmark with and thus SiO_2 is considered the standard. Simulations were performed for coupled microstrip line structures in Advanced Design System (ADS) environment by Keysight. Line-Calc was used to calculate the height of the dielectric required for impedance matching to 50 Ω and the values are given in Figure 20 (b). The impedance matching to 50 Ω is essential for ensuring lower reflections or discontinuity in the signal. A good impedance match also minimizes the reflected power.

Material A, B, and C are epoxy-based materials that are capable of fine-pitch RDL. Material D is a representative ultra-low D_k material. Simulation results shown in Figure 20 (b) demonstrates that Material D with the lowest D_k has the least dielectric height or effective polymer thickness, which means the signal-to-ground plane distance is the least in this material.

(a)



(b)

	E_r	D_f	H (um)
SiO_2	4		1.85
Material A	3.2	0.01	1.52
Material B	3.1	0.017	1.44
Material C	3.5	0.022	1.63
Material D	2.65	0.0008	1.32

Figure 20 Test Structures of Transmission lines used in the simulation

3.1.2.2 Effect of dielectric constant on crosstalk

Crosstalk becomes important when the spacing between the traces is reduced as in fine-pitch features. Crosstalk can cause coupling between interconnects, induces jitter in the system and can upset circuit logic. This is primarily attributed to the mutual inductance and capacitance between the conductors. In this analysis, a single aggressor and victim line was used. A time-domain source with an input pulse from 0-2.5V with 0.1 ns rise time, 0.1 ns fall time and 2 ns period was simulated using transient analysis for 100 ns with a time step of 1 ps for all 4 material candidates and the baseline. All ports were terminated with a 50 Ω resistor to minimize crosstalk because of reflections and line lengths were held constant at 5mm. The substrate properties were taken from Figure 20. The effect of the near-end (NEXT) and far-end (FEXT) crosstalk is shown in Figure 21 It can be seen that the FEXT values for Material D is significantly lower than the baseline case. The value of the FEXT is expected to fluctuate with changes in rise time, simulations at 10ps, 50ps and 0.1ns were run and the same trend of lower crosstalk was observed for Material D as compared to the Baseline. This shows the potential for lower crosstalk when moving towards low D_k materials for high-density RDL wiring requirements.

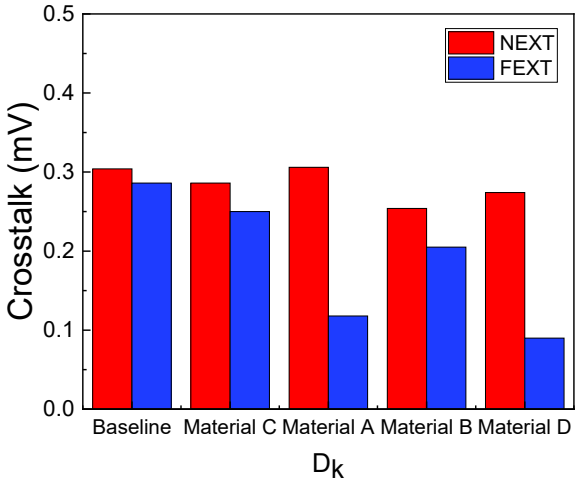


Figure 21 Crosstalk for dielectric candidates

3.1.2.3 Effect of material properties on signaling data rates

The primary motivation for choosing RDL materials with low D_k is their potential to signal at higher data rates while maintaining signal integrity. This along with fine-pitch routing lines will increase the overall bandwidth.

An eye diagram is a graphical tool that is indicative of signal integrity and electrical performance. It can be used to measure the jitter and distortion of the signal. Of more importance here, is data-dependent jitter which is caused by many factors including inter-symbol interference (ISI), crosstalk, etc. Also, for an ideal eye-opening, the eye-height should be equal to the amplitude. However, noise will cause the eye to close. A threshold value can be set to determine if the eye height is acceptable depending on the designer's budget.

In this analysis, a coupled microstrip transmission line of length 5mm was analyzed using a channel simulation which is designed for rapid signal integrity analysis of linear channels. A PRBS input source was used for a rise time of 10 ps, with V_{high} of 2.5V. The connector was terminated at 50 Ω to

minimize reflection loss. A crosstalk driver was used that models both synchronous and random crosstalk which inherited properties from the source.

Data rates of 2 Gbps, 5 Gbps, 9 Gbps,10 Gbps, and 12 Gbps were studied for a D_k of 4 (SiO_2), 3.2 (Material A), and 2.65 (Material D). The properties of Material A are taken to be representative of all epoxy dielectrics although there may be some variation. Figure 23 shows the eye-height and the complete eye-diagram at three data rates for three material options. A threshold value of 20% of the V_{high} was used to determine eye-closure. At 10 Gbps, the eye-height for the SiO_2 and Epoxy are both below 2 V while the ultra-low D_k dielectric is at 2.025 V. This suggests that there is potential to signal at higher data rates when we use an ultra-low D_k material, as initially hypothesized.

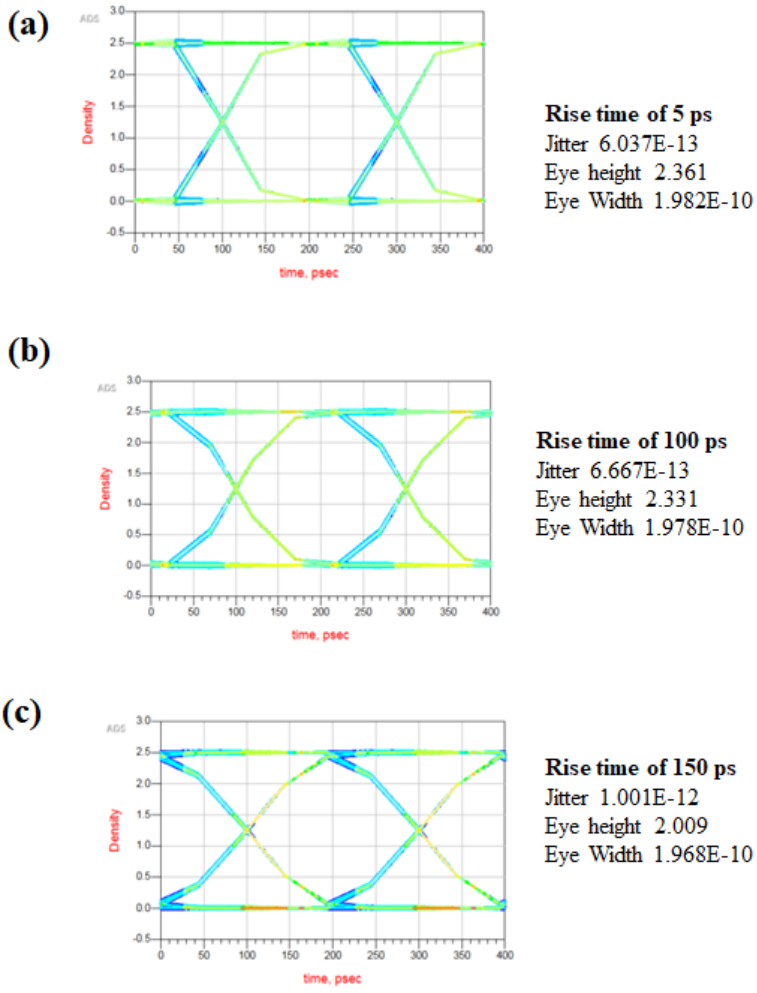


Figure 22 Effect of rise time on the eye height and jitter (a)5 ps (b) 100 ps and (c) 150 ps

However, the eye-opening is dependent on the rise-time of the source. To consider the impact of varying the rise-time, simulations were run at a fixed data rate of 5 Gbps and with rise times ranging from 5 ps – 150 ps for an epoxy material candidate. It can be seen from Figure 22 that a larger rise time decreases the eye-height to a huge extent but does not influence the jitter as much. It is expected that with a higher data rate, the effect of increasing rise time on jitter will be more significant. The eye height changes from 2.361 V to 2.009 V on increasing rise time. This indicates that the rise time effects are significant at data rates >=5 Gbps. The next consideration was the effect of line length on the eye properties. For this, we considered line lengths of 3 mm and 6 mm, which are within the range of the

expected length of connections between HBM-Logic devices. These simulations were run at 5Gbps with the same input source and a 10ps rise time for an epoxy material candidate. From Figure 24, we observe that the eye- properties change with increasing line length. Jitter and noise become worse for longer lengths as is seen from the reduction in eye-height and increase in jitter.

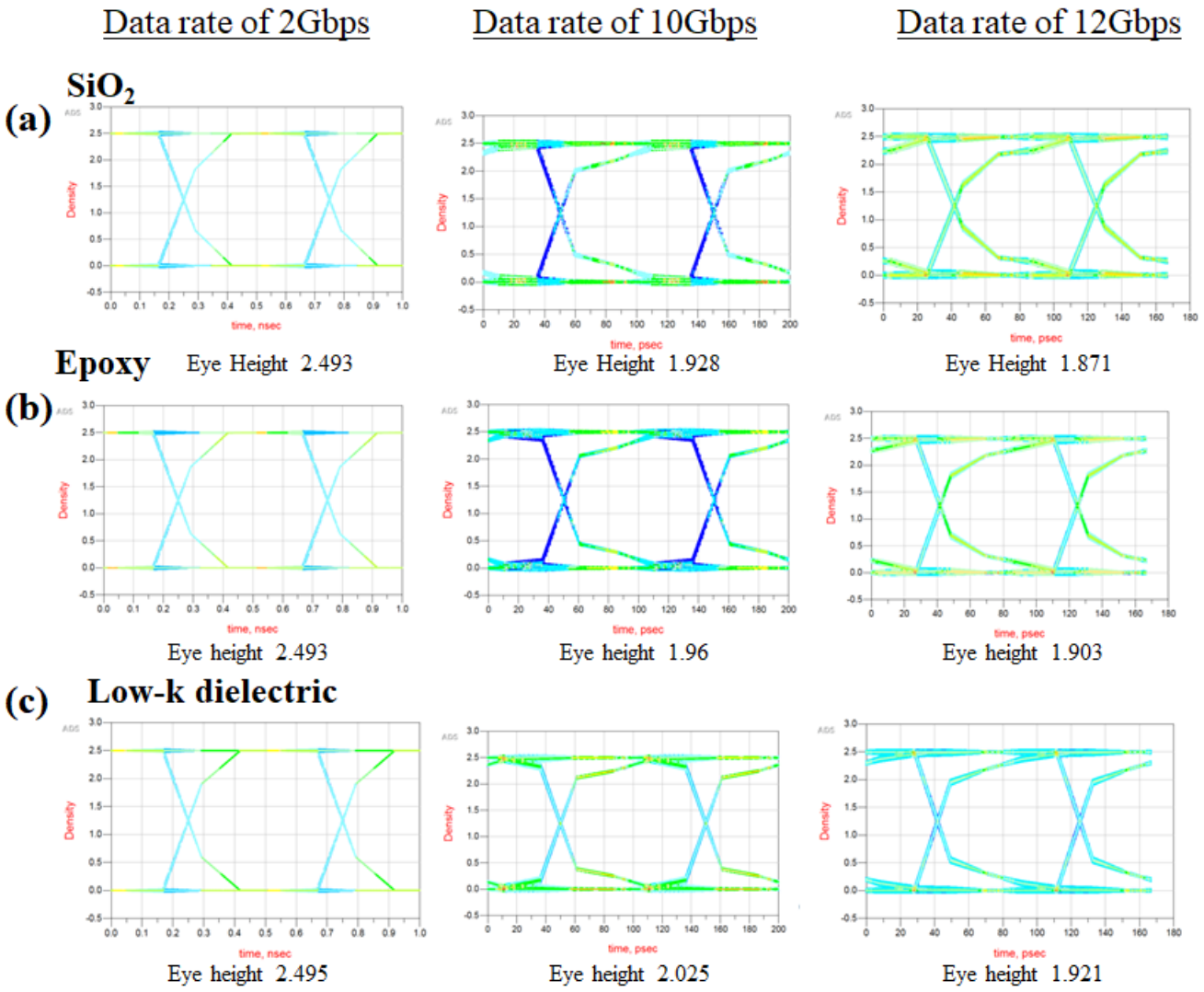


Figure 23 Estimated maximum data-rate for three dielectric material candidates

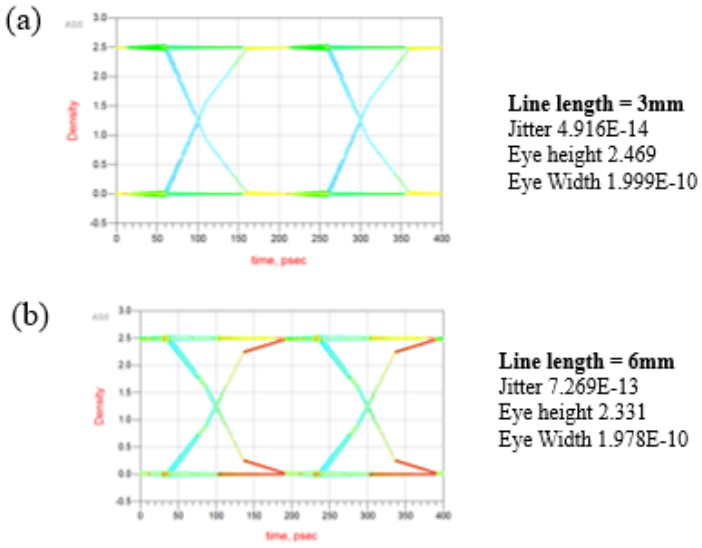


Figure 24 Effect of line length on eye properties (a) 3mm (b) 6mm for epoxy dielectrics.

To summarize, we have simulated the crosstalk between coupled microstrip lines for interposer-like design rules and analyzed the maximum data rate acceptable for given dielectric constant. The results indicate that there is at least a 10% reduction in crosstalk when you shift to a material with lower dielectric constant as compared to SiO_2. These values are expected to increase when you consider longer routing wires. The maximum data rate for signaling using a low dielectric constant was estimated to be around 10Gbps which overcomes the limitations faced by conventional high-D_k epoxy's and BEOL alternatives. This suggests that it would be beneficial to use low-D_k materials in the high-density routing layers. Current HBM-logic data rates are limited to 1-2 Gb/s as outlined by JESD235A standard as the data rate/pin, but it is expected to increase based on future requirements of linear bandwidth density of 10 Pb/s.m at the die edge.

3.2 Materials characterization

The previous section detailed the materials selection and presented preliminary results on the electrical design. This section describes materials characterization of ultra-thin, ultra-low D_k dielectrics. There are two parts in this section a) characterization of single microstrip transmission lines and b) characterization of insulation resistance

3.2.1 Characterization of single microstrip lines

In this section, test-structures to characterize the insertion loss are fabricated and measured. An epoxy-based material is used to fabricate test-structures and to validate simulation results. These measurements are used to demonstrate that these test-structures can be fabricated and to build confidence into the simulation set-up. Further, an advanced simulation structure is used to predict the bandwidth increase from using ultra-low D_k, ultra-thin dielectrics.

3.2.1.1 Fabrication of single microstrip lines

The test-structures were fabricated using a semi-additive process (SAP) which is described in detail in Chapter 4. A low TTV silicon wafer is used as substrate core. Denton discovery RF/DC was used to sputter a ground layer of 50 nm Ti/500 nm Cu. A 5 µm dry-film of ABF GXT61 was vacuum laminated onto the substrate. Vias were drilled using the picsecond UV laser tool to connect the ground plane to the measuring plane. A 7 µm dry-film PR from TOK was used as the photoresist to patten fine-features. The copper traces were plated up to a height of ~4 µm. Figure 25 shows the fabricated 3-5 µm single microstrip lines after seed-layer etch.

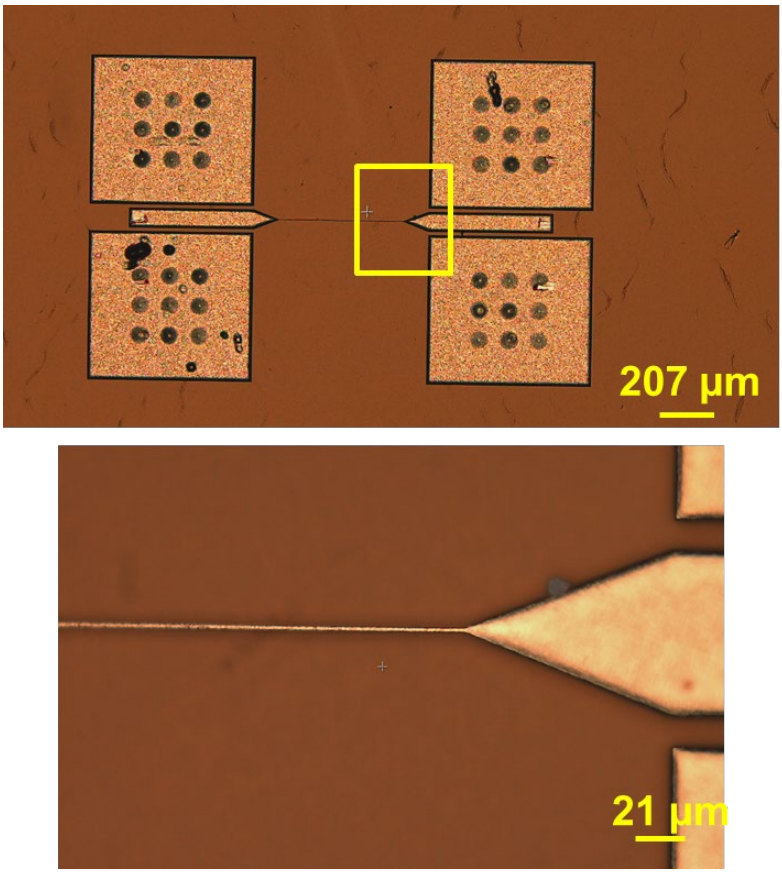


Figure 25 Fabrication of 3-5 µm microstrip lines

3.2.1.2 Insertion loss measurement of 3-5 µm microstrip lines

Microstrip transmission lines were characterized to build confidence into the 3D HFSS simulation model and material properties. This model was then used to predict the bandwidth increase because of ultra-low D_k and ultra-thin dielectrics. Different line-lengths of the same line width/space of the microstrip line were fabricated. L-2L de-embedding techniques were used to remove the effects of the pad and to calculate the insertion loss per unit line length. Figure 26 (a) shows the insertion loss for different line lengths for a 5 µm microstrip transmission line. The trend indicates that longer lines have a higher insertion loss than shorter lines. The 5 µm lines show better yield than 2-3 µm lines with very less variation in copper cross-section and hence, were chosen as the baseline structure to validate the model. In

characterizing such ultra-fine pitch structures, small process variations have an impact on the insertion loss [45]. Figure 26 (b) demonstrates the comparison between modeling and experimental measurements for a microstrip transmission line. The model shows good co-relation to the experimental results up to 7 GHz. The insertion loss is <1.5 db at 8 GHz.

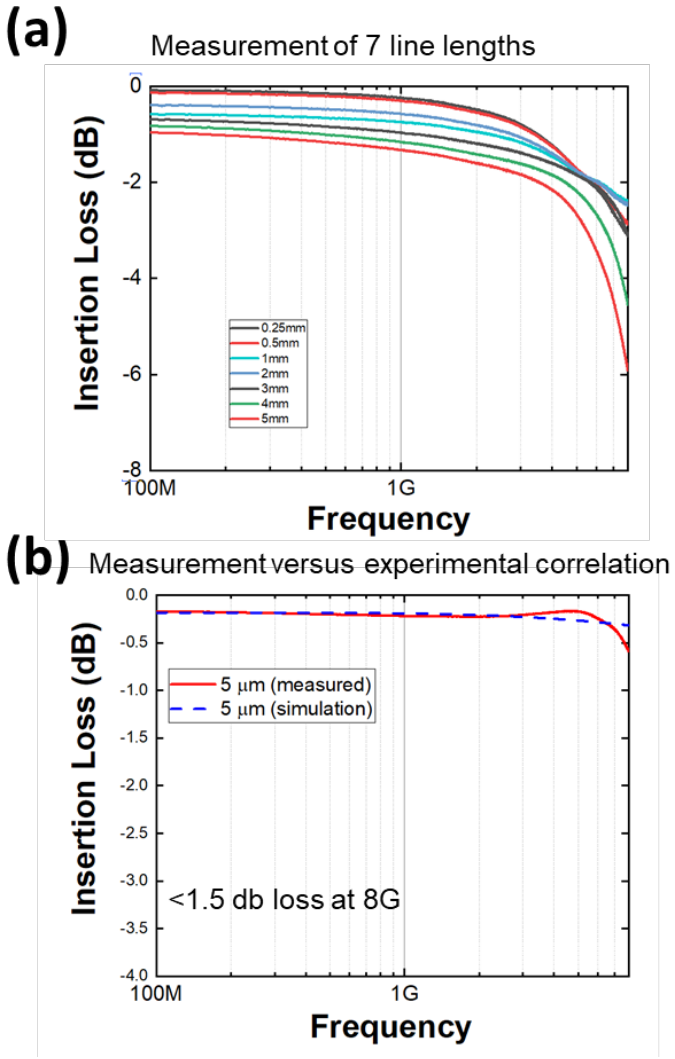
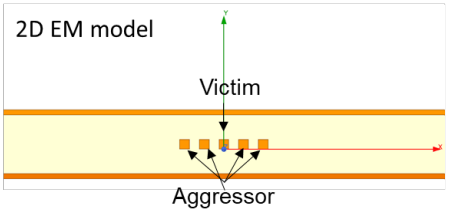


Figure 26 S_{21} of microstrip transmission lines (a) experimentally characterized for different line lengths (b) experiment versus simulation comparison for per unit mm of line length

3.2.1.3 Bandwidth improvement realized using ultra-low D_k and ultra-thin dielectrics

In order to understand the impact of dielectric constant on the overall bandwidth of the system Figure 27 (a) was designed in Ansys HFSS. A structure with stripline transmission lines using four aggressors and one victim was used to mimic an aggressive model for interposer-like signaling. Impedance matched dielectric thickness for different dielectrics was used as shown in Figure 27 (b). A constant IO density is maintained by not varying the line width/space. The I/O density used is 250 IOs/mm/layer. Simulated eye-diagrams which take into account the crosstalk between all the aggressors is shown in Figure 28. At higher data rates of 16 Gbps the eye almost closes when using a D_k of ~4.0, while there is still potential to signal using an ultra-low polymer dielectric. Taking an eye-height of 0.7 V as threshold voltage, the maximum data rate for a given dielectric constant is calculated and shown in Table 6. The bandwidth is calculated as a product of wiring density (250 IOs/mm/layer) and the data rate for each dielectric. A ~35% increase in bandwidth is demonstrated using an ultra-low D_k dielectric over an inorganic dielectric.

(a)



(b)

Material	D_k	D_f	Ground plane spacing (µm)
Ultra-low D_k	2.5	0.005	6.95
Epoxy	3.2	0.01	8.23
SiO_2	4.0		9.84
Width 2 µm, length 5 mm, height 2 µm			

Figure 27 (a) Test-structure for channel simulation (b) Material properties of the dielectric

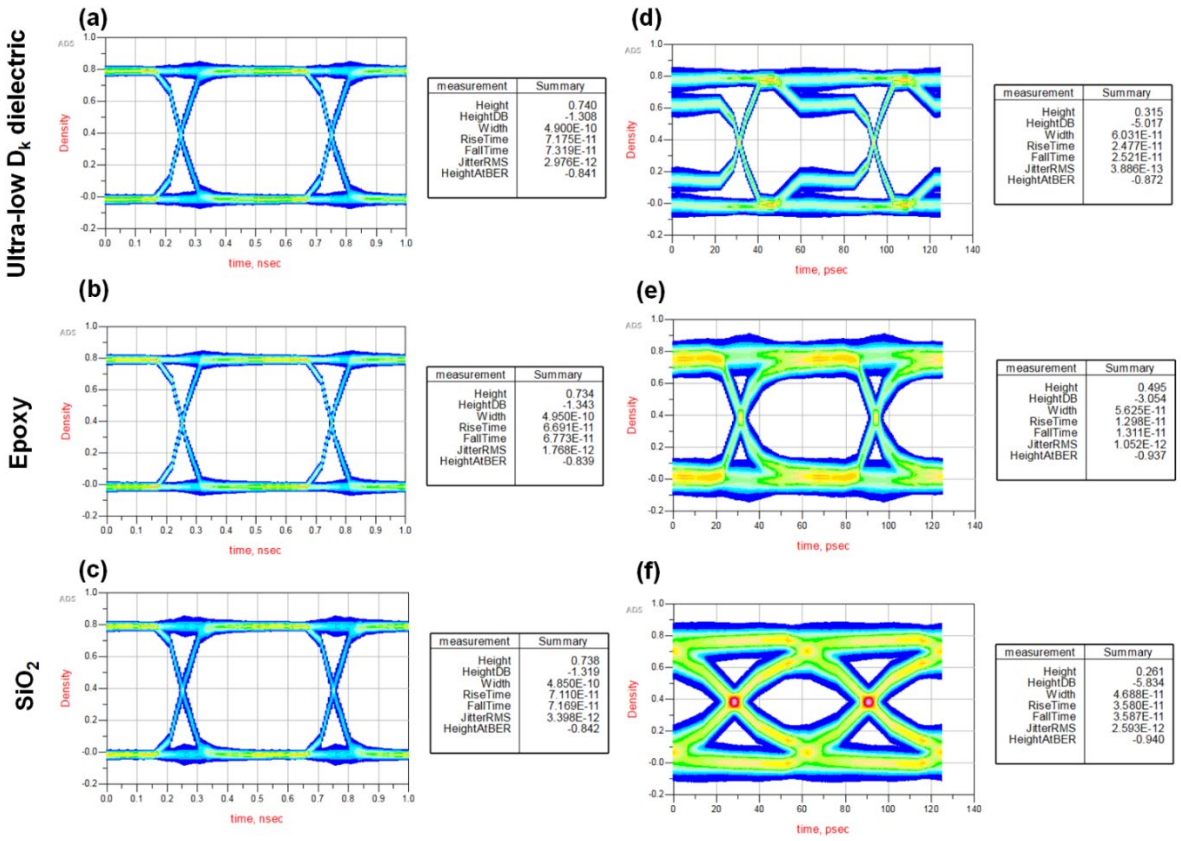


Figure 28 Simulated eye-diagrams for impedance matched stripline with multiple aggressors and one victim (a),(b) and (c) are at a data rate of 2 Gbps and (d), (e), and (f) are at a data rate of 16 Gbps.

Table 7 Maximum data rate for a given dielectric constant. Bandwidth is calculated for a given wiring density of 250 IOs/mm/layer.

	Data Rate	**Bandwidth**
Ultra-low D_k dielectric	4.84 Gbps	1.21 Tbps/mm/layer
Epoxy	4.3 Gbps	1.075 Tbps/mm/layer
SiO_2	3.6 Gbps	900 Tbps/mm/layer

3.2.2 Insulation resistance of ultra-thin dielectrics

Ultra-thin dielectrics reduce the distance between the electrodes and thereby increase the potential for shorting due to electrochemical migration. Moisture absorption in organic materials such as polymer dielectrics is often the failure mechanism which eventually results in dielectric blistering because of hygroscopic swelling, package cracking because of interfacial failure or copper electrochemical migration [46, 47]. There has been work to prevent copper electrochemical migration using an inorganic barrier [48]. But, the insulation reliability of the polymer dielectrics under aggressive test-conditions has not been studied. In this study, the effect of highly accelerated stress test (HAST) on the polymer is evaluated.

3.2.2.1 Fabrication of test-structure

The material properties of the dielectrics used in this study are given in Figure 29 (a). These represent different dielectric material classes such as epoxy, benzocycobutene (BCB) and phenolic resins. The dielectric thickness used was 5 μm. The moisture absorption is <2 wt.% for all material candidates. These materials represent advanced polymer dielectrics capable of high-density (< 2 μm SAP RDL) interconnects. The ionic content of the polymer dielectrics influences the leakage current. However, considering that all the material candidates have very low fluorine and other halogenated ions, the effect of ionic impurities is neglected. Of all the three materials, material B has the least moisture absorption of <0.2 wt.%.

A capacitor test-structure was used to measure the leakage current as shown in Figure 29 (b). A silicon wafer of 0.5 mm thickness was used as the substrate. A ground layer of 50 nm Ti/300 nm Cu was sputtered using the Denton RF/DC sputter tool at a deposition rate of 3.5 Å/s. The dielectric was deposited using either vacuum lamination or spin-coating followed by cure at the recommended temperature. A mask with 2 mm X 2 mm cut outs was used to evaporate 450 nm aluminum using the denton explorer e-beam

evaporator. The test-structures were placed in a HAST chamber at 130 ºC, 85% RH for 96 hours and the leakage current was measured before and after testing.

(a)

		Material A	Material B	Material C
Chemical	Curing temperature	171 °C	210 - 250 °C	<200 °C
	Moisture Absorption	0.6 wt.%	< 0.2 wt.%	-
	Film-type	Dry-film	Liquid	Liquid
	Thickness	5 µm	5 µm	5 µm

(b)

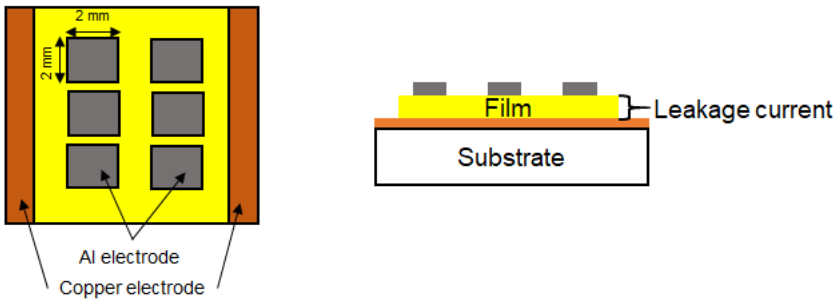


Figure 29 (a) Material properties of the polymer dielectrics (b) Schematic of capacitor test-structure

3.2.2.2 Leakage current

The leakage current measured before and after HAST for all three dielectrics is shown in Figure 30. All three dielectrics show the same overall trend for before and after HAST current ranges from -100 V to 100 V. All dielectrics survive the aggressive HAST test and do not show a very high increase in leakage current. The range of voltage expected for high-performance computing applications is -5 V to 5 V and we see that within that range the leakage current is < 1E-08 which is a ~10% change. The material with the least moisture absorption material B showed the least change before and after HAST although the

other dielectrics are in the same range. This study shows that all ultra-thin dielectrics with < 2 wt. % moisture absorption will survive aggressive humidity and high-temperature environments.

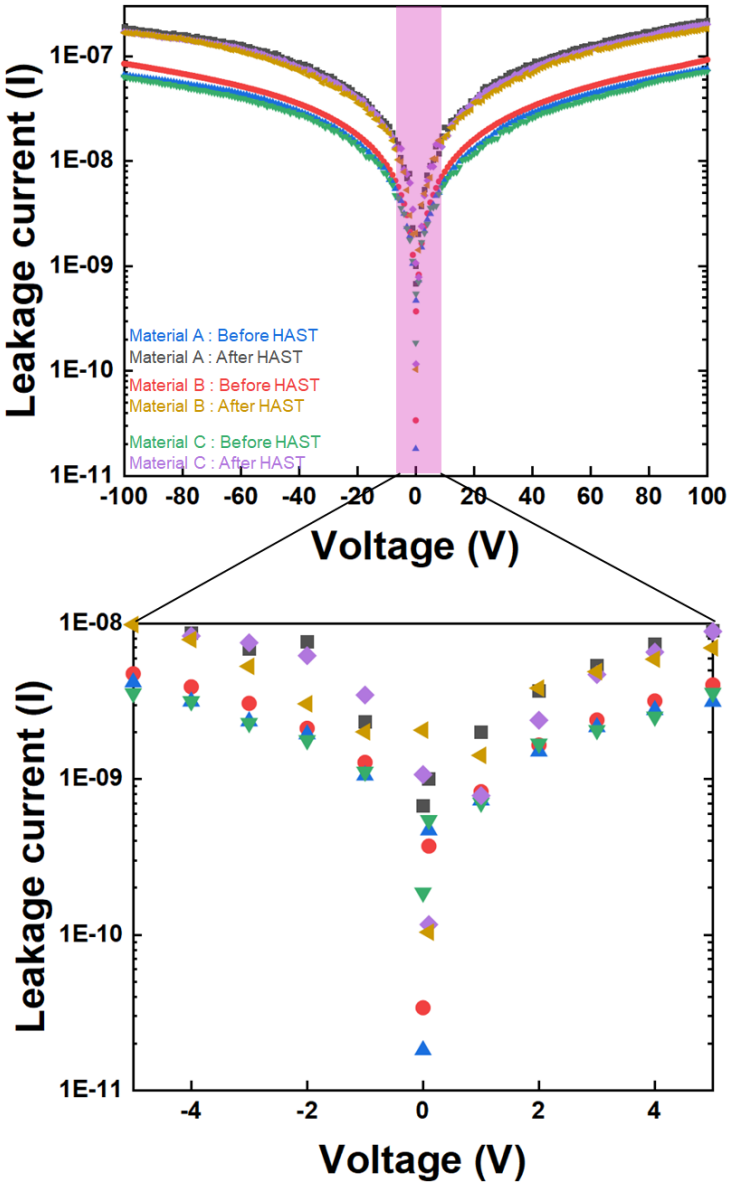


Figure 30 Leakage current before and after HAST. The colors represent the test-conditions. For before HAST conditions: blue, red and green present material A, B and C. For after HAST conditions: grey, yellow and pink represent material A, B and C. The figure below is zoomed in from the figure above to show the trends between -5 V and 5 V

3.3 Chapter summary

This chapter described the upfront materials selection criteria that will be used throughout this thesis. The three material classes selected were epoxy, BCB and phenolic resins. These materials present an optimal mix of electrical, physical, mechanical and chemical properties required for next-generation high-density RDL. Appropriate material candidates in these material classes will be selected in experiments through this thesis. Next, this chapter looks at the design, fabrication and characterization of high-density RDL using ultra-low D_k materials. It identifies a potential to signal up to 10 Gbps for low D_k materials. This proves for the first time that for the same wiring density, organic RDL with ultra-low D_k, ultra-thin polymers offer the potential to increase bandwidth by 1.5X and reduce power consumption. Further, this chapter also looks into the insulation reliability of the selected material candidates before and after HAST. No significant leakage current increase is observed in the range of interest for these materials, further improving their potential as material candidates for next-generation RDL.

CHAPTER 4. PROCESSES FOR ULTRA-THIN DIELECTRICS

Current advanced packaging substrates use thin-film polymers of >15 μm dielectric thickness. This chapter discusses research to push the limits of advanced RDL to < 2 μm dielectric thickness for better electrical performance as described in Chapter 3. The critical steps identified to meet this need are a) deposition of ultra-thin dielectrics and fabrication of fine-pitch structures b) evaluating the surface planarity for advanced dielectrics. This chapter has two sections to present advances in these two areas. The material selection picks from the material classes identified in the previous chapter. The first section will present process advanced and demonstrate ultra-fine pitch structures with ultra-thin, ultra-low D_k dielectrics. The second section will evaluate the surface planarity for these fine-pitch structures after coating a second polymer dielectric layer using the processes described in the first section. Further, an optimal processing window is identified for creating planar surfaces and additional planarization steps are explored.

4.1 Deposition of ultra-thin dielectrics and fabrication of fine-pitch structures

In this section, the process optimization done to fabricate fine-pitch line/spaces with ultra-low D_k, and ultra-thin dielectrics is discussed. The process flows used are introduced in the technical approach followed by the key material and tooling requirements needed to optimize the process is described. Finally, the fabrication results with low-D_k materials is shown.

4.1.1 Technical Approach

Traditionally semi-additive-processes (SAP) have been used to pattern re-distribution layer dielectrics (RDL) to below 5 μm. There are several challenges to patterning below 3 μm such as a) seed-

layer etch b) photo-resist resolution for controlled line width and space. In contrast to prior work on silicon wafers for wafer-level-packages, this work looks at demonstrates ultra-fine lines using dry-film photoresists and panel-scalable processes on thin glass substrates. The standard SAP process flow schematic is shown in Figure 31 where a polymer thin-film is deposited onto the substrate followed by seed layer metallization and then lithography to resolve 2 µm line/space. Finally, electroplating and then seed-layer etching is carried out to fabricate the fine lines. This work looks at the extent to which SAP can be used to fabricate 2 µm lines on our upfront selection of ultra-low D_k material candidates.

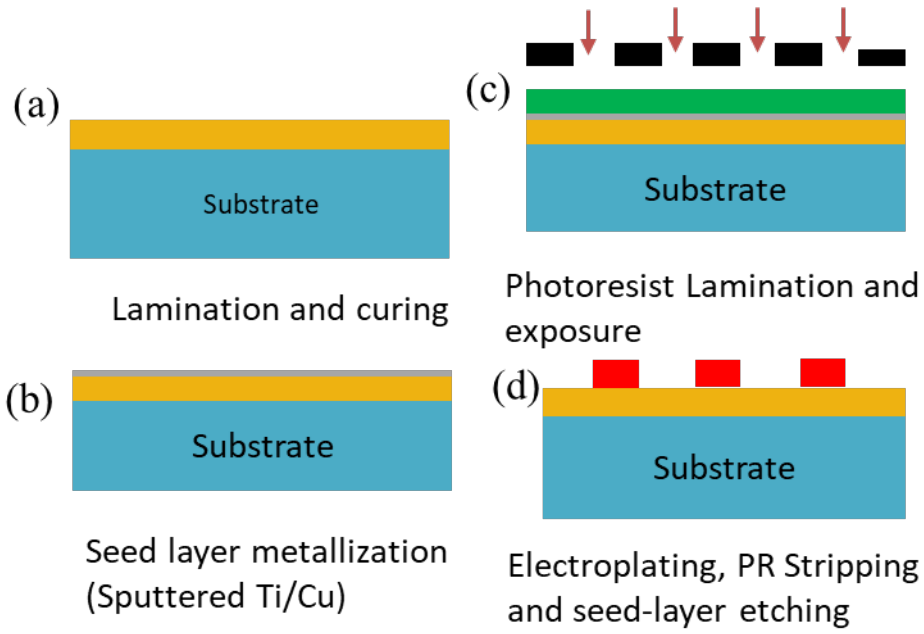


Figure 31 Semi-additive process to pattern RDL dielectrics

SAP is limited in scaling to < 5 µm vias as typically these vias need laser ablation. Suzuki, et.al have shown 10 µm vias in polymer dielectrics with an excimer laser ablation process [49]. Other work have also shown < 5 µm vias in polymer dielectrics with novel cleaning processes to ensure good side walls [50]. Microvia scaling and reduction in the capture pad dimension are critical to achieve the target wiring density. Photo-sensitive dielectric materials known as PIDs have the potential to form vias of < 5

µm without laser ablation. Further, the patterning steps can also be eliminated if lines/spaces or "trenches" could be formed on the dielectric. Based on this idea, the embedded trench based process was developed and the process flow in shown in Figure 32. Here, the dielectric material is laminated on the substrate and patterned using a photo-patterning tool. The PID is then cured after development to create fine lines/spaces. Sputtered Ti/Cu is used as the metallization followed by electroplating to build up the traces to the appropriate height. Fly-cut planarization, a CMP type process is used to remove the overburden copper as well as smoothen the surface for the next layer. This process will be explored to create < 5 µm vias and 2 µm line/spaces using the material candidates selected upfront.

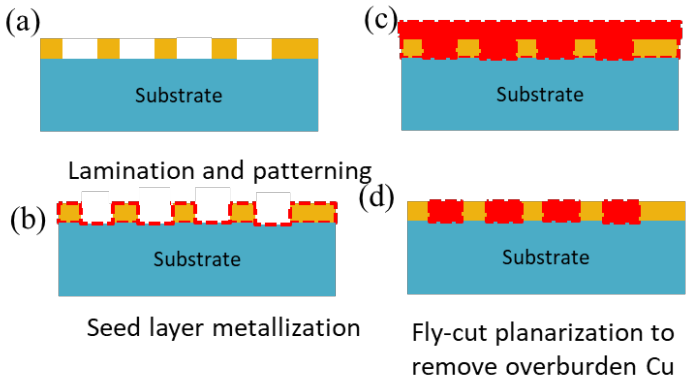


Figure 32 Schematic of embedded trench process

The deposition process that can be used to deposit ultra-thin dielectrics are outlined in Table 7. The advantages and limitations of each are discussed.

Table 8 Deposition processes for ultra-thin polymers

	Vacuum lamination	**Spin Coating** [51]	**Spray Coating** [52] [53]	**Slit coating** [54]	**CVD** [55]
Thickness	> 5 µm	> 0.2 µm	> 5 µm	> 10 µm	> 0.5 µm
Critical parameters	• Vacuum time • Pressure time • Temperature	• Polymer concentration • Viscosity	• Viscosity • Polymer concentration	• Viscosity • Polymer concentration	• Polymer chemistry
Application	• Photoresists • BU dielectrics • Prepreg	• ULT dielectrics • Photoresist	• Flexible electronics • Cu etch	• Dielectric material s • Photoresist	• Paralyene
Advantages	• Panel scale (500 X 500 mm) • Dry film	• Can deposit < 2 µm thickness	• Conformal • Versatile	• Panel scale	• Conformal • Panel scale
Limitation	• Challenging to move to < 5 µm	• Damascene process needs CMP • Not panel-scale • Liquid	• Very poor planarity • Not panel scalable • Liquid	• Challenging to move to < 5 µm • Thickness control • Liquid	• Pinhole defects • Poor planarity • Vacuum equipment

4.1.1.1 Material and tooling requirements

The key process steps involved in fabricating < 2 µm line/spaces and < 5 µm vias in the material candidates selected upfront involve optimization of a) dry-film photoresist or photo-imageable dielectric resolution b) lithographic tooling. Positive photoresists (PR) are seen to have better resolution capability and aspect ratio compared to negative photoresists [56]. Typically, in the printed circuit board (PCB) industry, dry-film negative tone photoresists are used. High resolution DFR with thicknesses of 5 µm and 7 µm have been developed by Hitachi Chemical and they have been shown to pattern < 3 µm traces [57]

. Other positive tone liquid PRs have been used to pattern < 1 μm [58]. A dry-film photoresist (DFR) from TOK PC-0449W-F8 was used to pattern traces in the SAP process. This film is 7 μm thick and can be used for patterning ≥ 1.5 μm. Typically, for fabricating < 1 μm traces using SAP the photoresist (PR) is optimized for an opening of 1-1.5 μm to compensate for the Cu over etch during seed-layer etching and maintain the line shape of the traces. The dry-film PRs or the PIDs are typically in a sandwich three-layer structure with polypropylene as the cover film and polyethylene terephthalate (PET) as the carrier film. For lithography, traditionally projection stepper tools are used which projects the patterns on the object plan (mask) to the image plane (photoresist) through a lens system. Typically, a 365nm wavelength of different numerical apertures (NAs) are used in production. The Ushio UX-44101 i-line (365nm) with an NA of <0.16 is used in this work. Although stepper tools are preferred in the industry because of the high throughput and reliability, the requirement of a glass mask with fine features makes it difficult to modify and fabricate structures. The Heidelberg MLA150 maskless aligner which is a direct-laser-write tool overcomes this limitation of requirement of a photomask and hence has been used in this work. The minimum feature size is < 1 μm and it has an exposure window of 150 X 150 mm^2. The MLA uses fiber coupled diode lasers for exposure and it applies a raster scan to generate the pattern with the substrate fixed in vacuum [59]. The drawback of this tool is the low throughput of the direct-laser-write, however the process flow established on this tool is directly transferrable to an i-line stepper tool.

4.1.2 Process development

The key fabrication process flow for Material D is shown in Figure 33. Here, the substrates were treated with silane (AP3000) to make the surface more hydrophilic. A vacuum hot-press was used to laminate the dry-film polymer dielectric to the substrate. Lamination is completed by first generating vacuum for 90s and then hot-pressing at 0.6MPa for 30s at 100 ^{0}C. The polymer was cured at the recommending curing temperature. The seed-layer metallization, with a stack of Ti/Cu, was performed

using the Denton Discovery RF/DC Sputtering tool. The sputtering parameters were controlled to reduce interfacial stresses from delamination [36]. The samples were annealed for 30 mins at 150 ^{0}C. They were patterned for the high-density features using a stepper panel-scale lithography tool. The samples were electroplated up to the required height using a commercial Cupraacid bath provided by Atotech. PR was stripped using a TMAH-based stripping solution followed by O_2 plasma to remove PR residue from between the traces. The samples were annealed for 30 minutes at 150 ^{o}C. The seed layer was etched using a differential seed layer etching tool.

(a)

	Process	Condition
1.	Adhesion Promoter (AP 3000)	Spin coated (3000 rpm, 20s, 120˚C/120sec)
2.	Vacuum Lamination	100 C, 90s vaccum, 30s pressure (0.6MPa)
3.	Post-Lamination Exposure	20 s UV cure
4.	Baking	90 C, 90s
5.	Curing	250 C, 1 hour (N2 oven)
6.	Argon Plasma	10 mins
7.	Sputtering	50nm Ti/150 nm Cu at low pressure
8.	Annealing	150 C, 30 mins
9.	PR Lamination	TOK 7um resist
10.	Exposure	Ushio Projection Litho
11.	Plating	2 um copper
12.	Annealing	180 C, 30 mins
13.	Stripping	60 s, 10 mins
14.	O_2 plasma	10 mins
15.	Seed etch	65 inch/min, RT

(b)

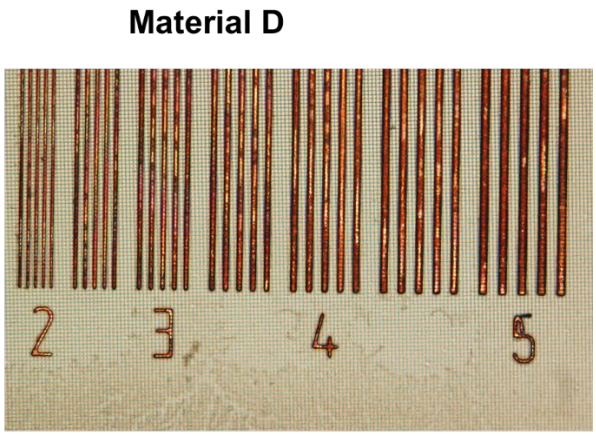


Figure 33 a) Process flow for fine-pitch RDL using SAP (b) 2 µm line/spaces on an ultra-low D_k dielectric (BCB)

The fabrication process flow for photopatterning Material D is shown in Figure 34. The exposure does was varied from 200 – 1150 mJ/cm^2 for different thicknesses of the dielectric and the results are as given.

(a)

	Process	Condition
1.	Adhesion Promoter (AP 3000)	Spin coated (3000 rpm, 20s, 120˚C/120sec)
2.	Lamination	Spin coated 14POO5 (1500 rpm, 20s, 90 ^{0}C/90sec)
3.	Exposure conditions	a) Ushio – 300-600 mJ/cm2
		b) Heidelberg – 200 – 1150 mJ/cm2, defocus of -2 to 2
5.	Development	30-60s DS 2100 puddle followed by 30s,1000 rpm spin with 10s fresh DS 2100 rise and 20s,2000 rpm spin to dry
6.	Post Develop Bake	90 ^{0}C, 60sec
7.	Cure	250 C, 1 hous

(b)

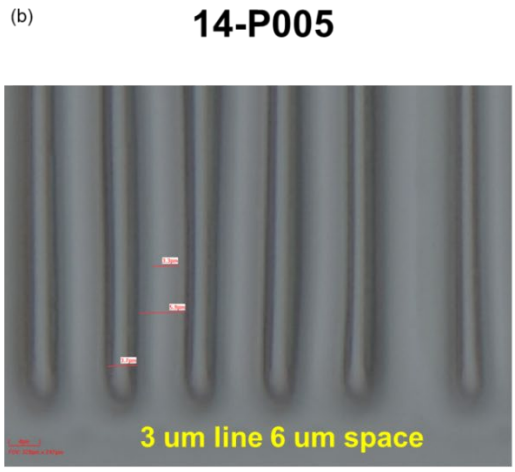


Figure 34 (a) Fabrication Process Flow and Conditions for fine-pitch RDL using a PID (BCB) (B) 3 µm lines patterned on a photo-sensitive polymer

4.2 Planarity for ultra-thin dielectrics

Fabrication of ultra-fine pitch structures requires each layer to be planar before the photoresist is coated and imaged. However, with smaller feature sizes and decreasing dielectric thickness there is a tighter window on the planarity of the substrate. Currently, stepper tools with an NA 0.18 can tolerate a DOF variation of 5 µm for a line/space of <1 µm [60]. The non-coplanarity is driven by four factors a) thickness variations across the panel or wafer (initial TTV) b) feature height variation c) substrate warpage and d) planarizability of the polymer dielectric. The viscosity of the polymer and coating parameters often determine if the film will "tent" or completely fill the gap between the copper traces. Several process variations have to be carried out to press the material using an optically flat surface to coat between fine-pitch traces. If not, additional cost-intensive process steps such as fly-cut planarization or chemical-mechanical-polishing (CMP) have to be used to smoothen the surface to pattern fine-pitch layers. Prior work has looked at spin-coated dielectrics for features of > 25 µm and observes that film shrinkage during cure and spacing of the features are important considerations for good planarizability [26].

The surface planarity for ultra-thin (<10μm) polymer dielectrics over copper wiring has not been studied. This work looks at establishing a methodology to fundamentally characterize the surface planarity for high-density RDL structures using an ultra-thin polymer. The technical approach describes the methodology for the experiment, the test-structure design illustrates the key problems being looked at and the process flow describes the key process parameters that have to be optimized to ensure smooth surfaces with ultra-thin polymer dielectrics.

4.2.1 Technical Approach

This work looks at characterizing the degree of planarizability using a laser confocal microscope. The working principle of the laser confocal is as given in Figure 35. It offers several advantages over traditional optical microscopy such as the ability to control the depth of field by using point illumination and a pinhole to eliminate out-of-focus signal instead of flooding the entire specimen with the light source. Light very close to the focal plane can be detected, the image's optical resolution is much better than wide-field microscope [61]. A laser confocal enables additional advantages by being highly monochromatic. The Olympus OLS5000 microscope was used for characterization and it uses a 405 nm laser with a vertical resolution of 10nm. It can be used to image samples >0.02 μm and up to a depth of 25 mm. The field of view is 16 – 5120 μm, the maximum scan area using the 5X objective is 2.5 mm. A typical output is as shown in Figure 36 where output 1 correlates the optical image of the features with a height map and output 2 shows the reflections from non-identical surfaces as identified from the laser raster scan and is useful to quantify the height of the dielectric above the copper traces and the dielectric height above the gap area.

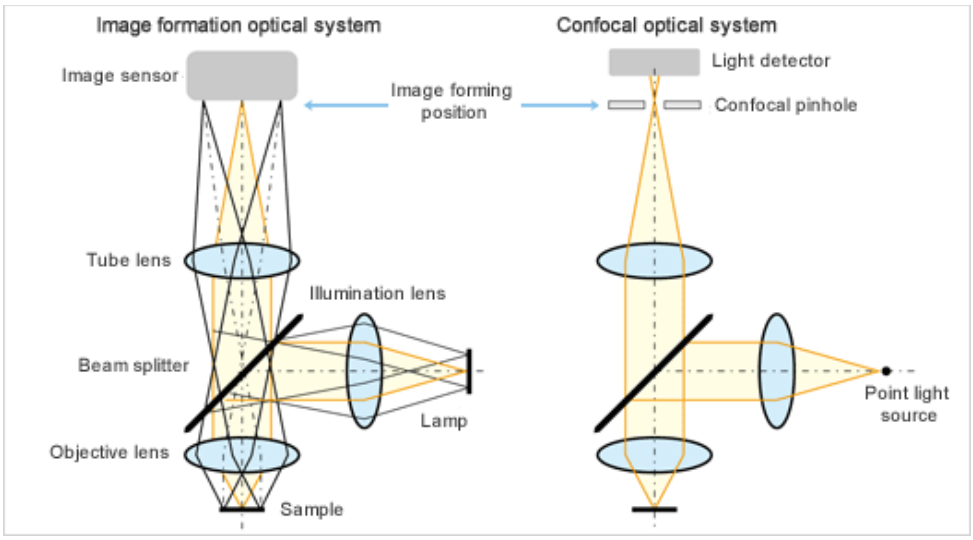
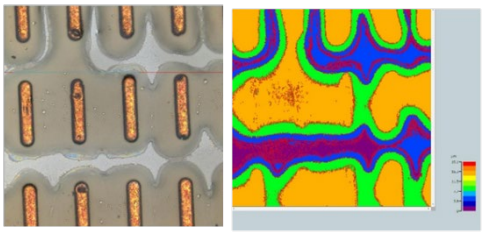


Figure 35 Working principle of laser confocal microscope

(a) Example Output 1: Height map corresponding to optical image



(b) Example Output 2: Laser image of reflections from non identical surfaces – thickness of polymer/copper

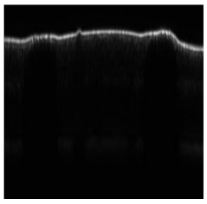


Figure 36 Output 1 corresponds to the height map from the image, Output 2 corresponds to the laser image of reflections from the substrate which helps determine the thickness of the polymer

4.2.2 Test-Structure

The process flow for fabricating and characterizing the surface planarity are as shown in Figure 37. These structures are fabricated on a 0.5-1mm thick silicon wafer with low TTV (through-thickness-variation) to ensure that substrate warpage does not have confounding effects with the surface planarity. The process flow involves lamination of the dielectric using a vacuum laminator with optimal conditions depending on the dielectric followed by seed layer metallization by sputtering 50nm Ti/ 150nm Cu on the wafer. A 15 µm DFR from Hitachi chemical is used for the test-structure shown in Figure 38 and a 7 µm DFR from TOK for the test-structure shown in Figure 39. This is followed by electroplating using a commercial plating bath from Atotech to the desired thickness and PR stripping using the specific chemistry depending on the DFR. Finally, a second layer of dielectric is laminated on the test structures and depending on the test-structure the thickness of the polymer is varied from 5-15 µm thick polymer. This is followed by a hot press step which is optimized using the different parameters. The material properties of the dry-film and liquid material candidate are as given in Table 8

Table 9 Material properties to evaluate surface planarity

		Material A (Epoxy)	**Material B (Phenolic resin)**
Electrical	D_k	3.2 (5.8 GHz)	2.8 (10 GHz)
	D_f	0.01 (5.8 GHz)	0.005 (1 GHz)
Physical	Thickness	> 5 µm	> 5 µm
	Film-type	Dry-film	Liquid

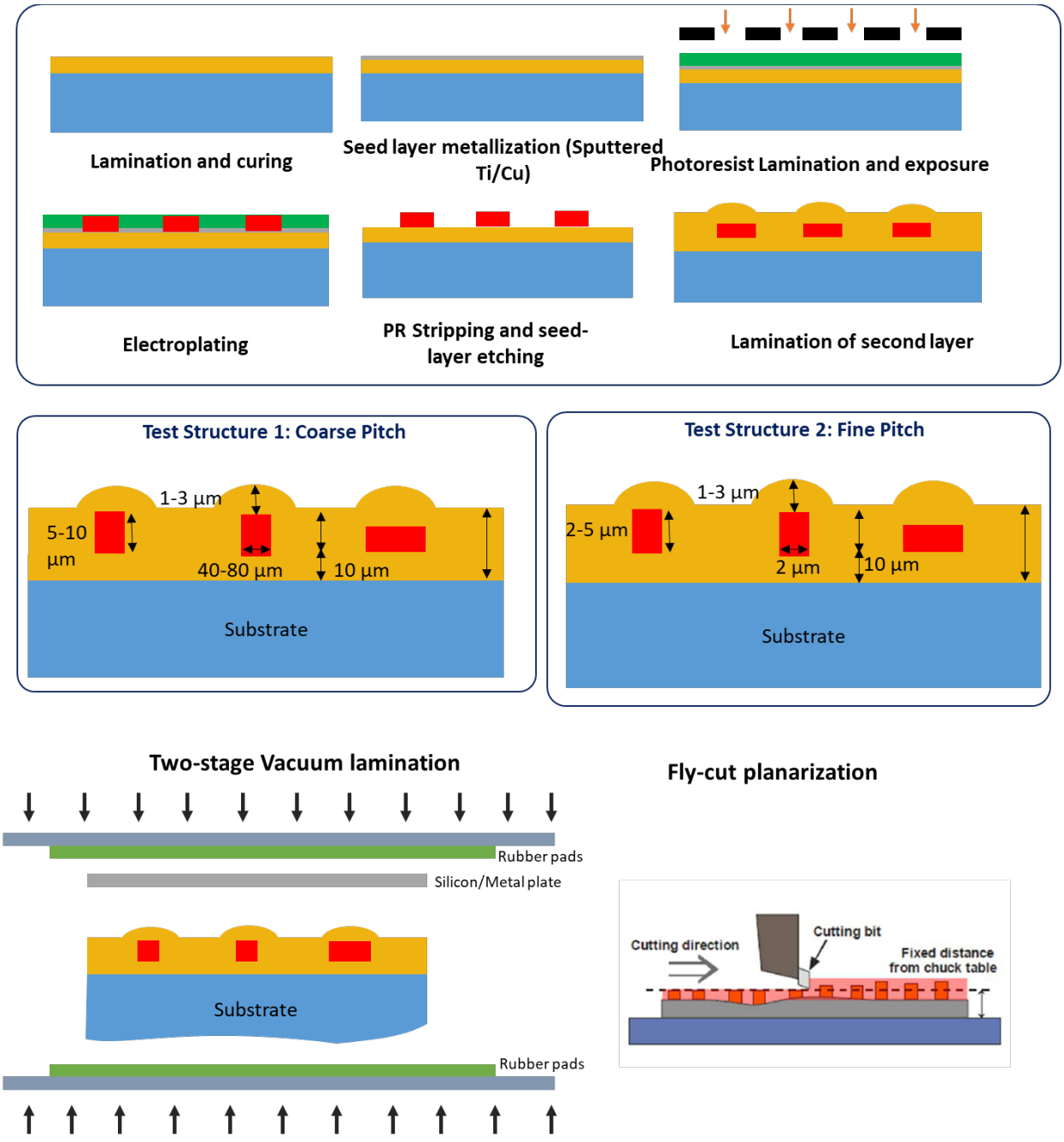


Figure 37 Process Flow for Fabricating Test-structure

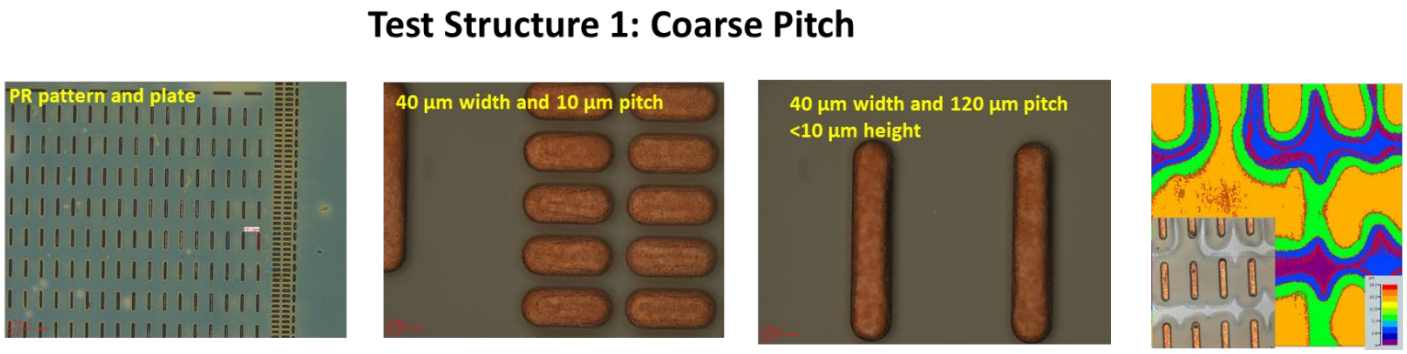


Figure 38 Test-Structure 1: Coarse Pitch RDL

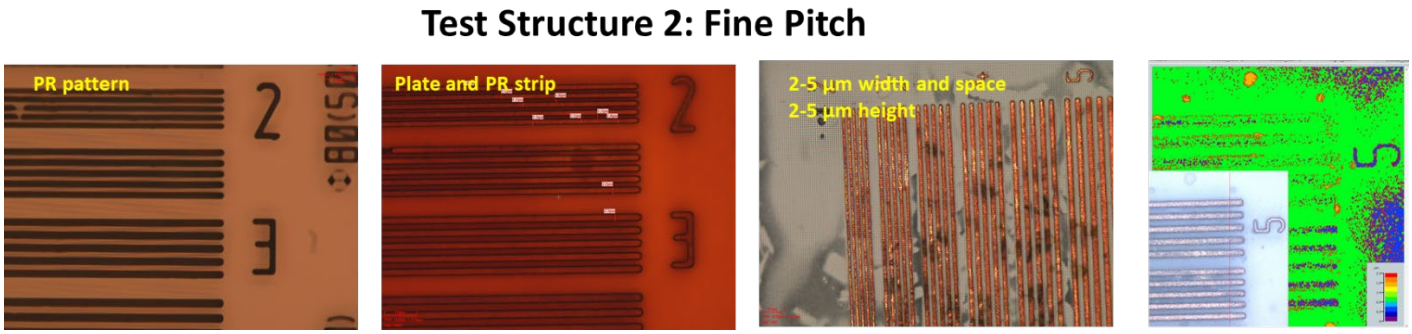


Figure 39 Test-Structure 2: Fine-pitch RDL

Dry-film deposition over a patterned substrate is done in a two-step process. The first step is to vacuum laminate it at a temperature of 100 ºC with 60 s of pulling vacuum followed by 0.6 MPa of pressure for 30 s. The second step is a "surface flattening" step which is carried out at the temperature of maximum viscosity of the polymer. The time, temperature and pressure of this flattening step have been varied to study their effect on the surface planarity.

The maximum tolerance of planarizability is limited by the resolution of the photolithography tool used to pattern the next layer and we have taken 5 µm as the cut-off.

4.2.3 Results and discussion

First, we examined the coarse pitch features or test-structure 1. Figure 40 (a) shows the surface planarity of test-structure A with material A. The dry-film thickness used was 15 µm and 5 µm. The vacuum pressure was varied between 0.4 MPa and 0.3 MPa. Increasing the pressure also increases the non-coplanarity for these coarse features. Lower pressures makes the polymer film tent over the copper structures and presents an appearance of co-planarity over the surface, however further inspection of the optical images indicate voids between the traces indicating that the polymer film has not filled the traces completely as can be seen in Figure 40 (c). Reducing the thickness of the dry-film from 15 µm to 5 µm results in an insufficient volume of material to fill the gaps as can be seen in Figure 40 (b). Thus, this study concluded that the thickness of the dry-film dielectric has to be matched to the feature sizes to ensure optimal dielectric height over the copper trace. Further, higher pressure during the two-step vacuum lamination process has an influence in improving the polymer flow between traces.

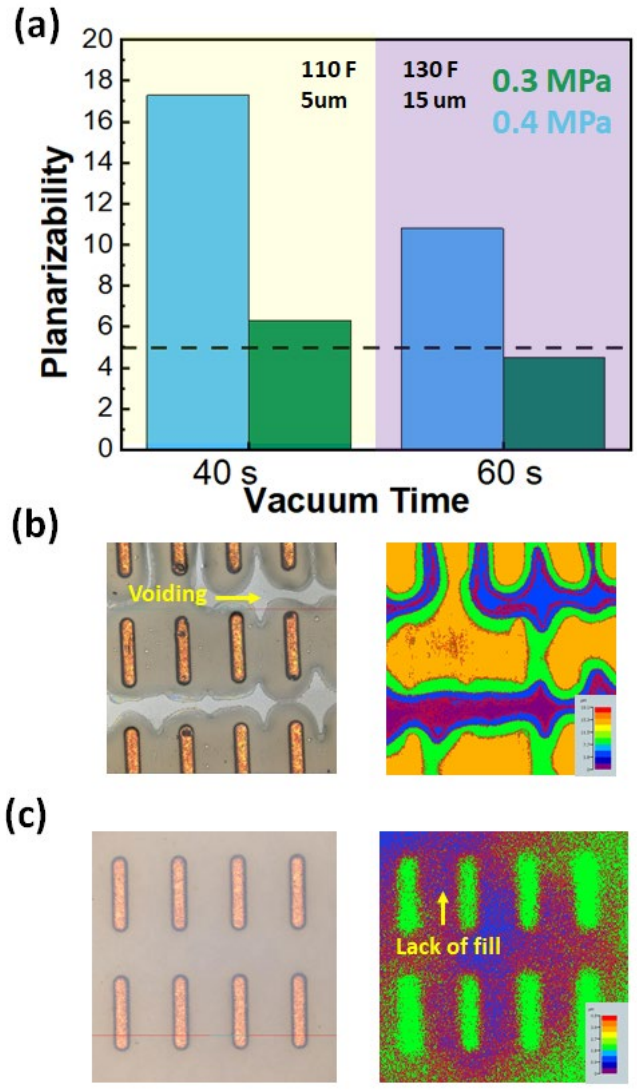


Figure 40 . Vacuum time, vacuum pressure, temperature of lamination and thickness of film were the factors to analyze planarizability for dry-film candidate. (a) Planarizability for vacuum times of 40 s and 60 s with test-structure 1. Optical and confocal height map for representative sample using a (b) 5 µm dielectric thickness (c) 15 µm dielectric thickness and 0.4 MPa vacuum pressure.

Next, we examined fine-pitch features, that is test-structure 2 as shown in Figure 39. The two-stage vacuum lamination process described earlier was used for Material A. The planarizability versus vacuum time for the pressure is plotted for different temperatures in Figure 41 (a). The increase in planarizability on higher pressure across vacuum times and temperature suggests that it plays a dominant role. Further, at higher temperature this effect is enhanced. Overall, two-stage vacuum lamination appears to work well

for fine-pitch features with the entire processing window being acceptable. Based on this study the best processing window was found to be 0.4 MPa pressure at 130 F for a vacuum time between 40 – 60 s. Spin coating was used to deposit the liquid Material B dielectric. The dielectric height and viscosity were varied to understand the planarizability of the dielectric before and after cure. Figure 41 (b) shows that almost all structures exceed the tolerance limit before cure. This can be attributed to the polymer flowing over the traces lacking rigidity to define or fill the gap. The polymer dielectric flows over the traces to completely cover them. On curing at elevated temperature, the polymer attains rigidity and capillary forces work to level out the surface. Figure 41 (b) shows that viscosity does not have an influence on the planarizability. All of these samples underwent similar temperature process cycles. Perhaps, in an aggravated elevated temperature cycle the effect of the internal shear forces might come into play but for substrate fabrication the density of the polymer solution did not have an effect. We can see that the thickness of the polymer has an effect on the planarizability. A dielectric thickness of > 5 μm is used for a copper height of 4 μm to maintain dielectric height over the copper. Comparing the structures with dielectric thickness of 2.5 μm and 5.5 μm suggests that taller copper structures are more difficult to planarize. There is a drive towards tall copper structures on polymer RDL to take advantage of potential lowered resistance [62]. From this study, we conclude that although liquid dielectrics allow a wider margin of control over dielectric height, they are limited in planarizability of tall copper structures.

Next, to improve the planarizability of liquid dielectrics a fly-cut planarization process was used [63]. Here, ~ 1 μm thickness of the dielectric was cut off. < 5 μm planarizability was achieved for liquid dielectrics with tall copper structures as seen in Figure 41 (c). Although this appears to be an ideal process option two limitations were noticed during process development a) the instrument does not take into account local planarity which makes it difficult to control dielectric height b) delamination between dielectric copper because of insufficient adhesion. Further, this step adds an additional step to the overall

fabrication process increasing cost and time. Hence, the use of the process for planarization of fine-pitch traces is limited to high-end application requirements.

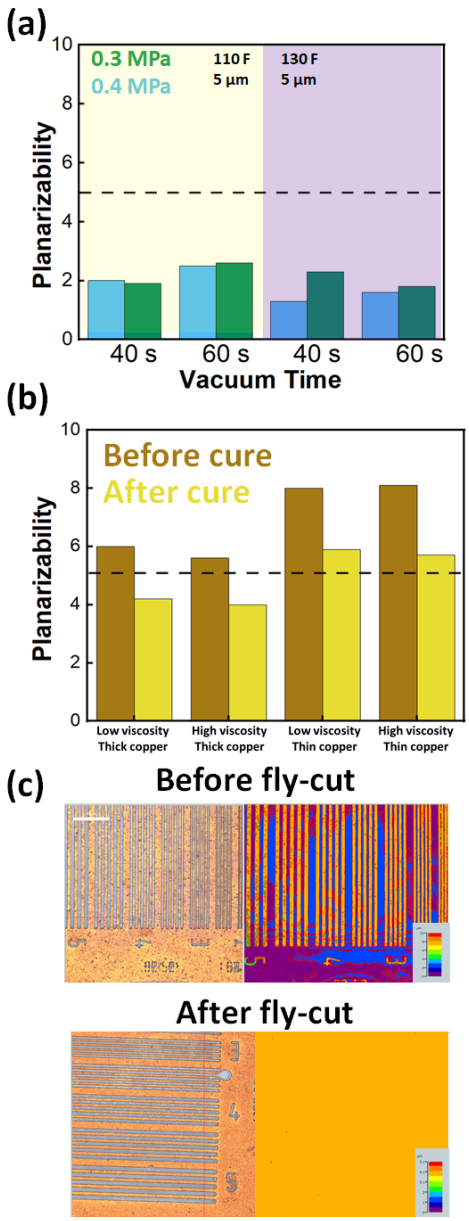


Figure 41 Planarizability versus processing conditions. Fine pitch structures with (a) Material A (vacuum lamination). The x-axis indicates the vacuum time for pressure at 110 F and 130 F. (b) Material B (spin-coated). The x-axis indicates the viscosity of the material used and target dielectric height. The dotted black line indicates the maximum allowable global planarizability.

4.3 Chapter summary

This chapter described the deposition and fabrication of ultra-fine pitch structures on ultra-thin, ultra-low D_k polymer dielectric materials. Fine-pitch structures are fabricated using traditional SAP process flows and advanced embedding approaches. Surface planarity with respect to coating a second layer of the dielectric in a panel-scalable process with highest degree of planarization is discussed. Ultra-thin dielectrics perform well after initial optimization of including a two-stage vacuum lamination process flow. However, the dielectric thickness cannot be controlled to achieve impedance matching for fine-pitch structures. Hence, ultra-thin, ultra-low D_k liquid dielectrics were studied for surface planarity for fine-pitch structures. Tall copper structures required an additional planarization step to improve the surface planarity. Thus, this chapter provides process guidelines for fabricating ultra-fine pitch structures with ultra-thin dielectrics.

CHAPTER 5. RELIABILITY OF ULTRA-THIN, ULTRA-LOW K RDL DIELECTRICS FOR FINE-PITCH WIRING

This chapter presents two aspects of ultra-thin, ultra-low D_k polymer dielectric reliability a) thermo-mechanical reliability b) chemical reliability. The first section will evaluate the effect of polymer dielectric material properties on the stress at the polymer/copper interface. The second section will investigate novel surface modification techniques to improve the adhesion at the polymer/copper interface. There is a clear emphasis on understanding and improving fundamental material structure to achieve reliable polymer/copper interfaces.

5.1 Thermo-mechanical Reliability

5.1.1 Multi-layer thermo-mechanical reliability

This section will explore the interfacial stress created by the difference in polymer and copper material properties in multi-layer interconnects or microvias.

5.1.1.1 Background and overview

Rapid increase in the number of devices connected to the network and the data generated by these devices, coupled with growth of know-how on the processing of this data with advanced machine learning and deep learning algorithms, has promoted a rising need to scale compute speed and capacity. Advanced packaging solutions which combine ultra-high bandwidth with low power interconnects with cost-effective manufacturability are gaining prominence [3, 13, 64-68]. As package technology becomes more wafer fab-like, achieving interconnect densities to support >1 Tbps on-package interconnects requires novel substrate capabilities [69]. A critical need is to improve packaging interconnect density and

performance. Ultra-high interconnect density is achieved by either increasing the number of lateral interconnects or vertical interconnects. There has been tremendous progress in pushing RDL dimensions of lateral interconnects down to 2-1 μm [6, 62] but there are significant unexplored challenges in scaling down vertical RDL interconnects or microvias.

Advancing microvias technology to smaller via and pad diameters allows for an increase in spatial routing area and helps meet next-generation heterogeneous integration needs for reduced bump pitch. The IO density versus microvia diameter needed to achieve the interconnect density is depicted in Figure 42. Typical organic high-density packages can support a maximum of 500 IOs/mm/layer [69]. Isotropic plasma etching processes was developed with high processing speed for via formation, similar to plasma RIE used in BEOL but large side etching makes it difficult to form vias < 75 μm [70]. Laser tools can be used to drill vias however, they form one via at a time using serial processes. CO_2 laser drilling supports high through put but is limited due to the long wavelength and large beam size and can support > 60 μm via diameter [71]. In contrast, UV laser uses a shorter wavelength and the current state-of-the-art via dimension is 20 μm diameter [21], although there have been reports of < 5 μm diameter using a picosecond UV laser tool [72]. Excimer laser ablation has been used in fan-out packages to create < 5 μm via diameter [73, 74]. Of increasing interest are photo-imageable dielectrics (PID) that can be patterned to ~3 μm via diameter. Further, PID materials can be employed in an organic dual-damascene process for fine-pitch < 1 μm lines and spaces, overcoming the challenge of SAP side-etch for less than 1 μm critical dimension [25, 62]. Thus, PIDs are promising candidates to meet next-generation interconnect needs. However, in terms of scaling down the via diameter using PIDs or other laser tools there exists a significant gap in knowledge, the reliability of < 20 μm via diameter has not been studied [75]. There is a need to understand the geometry design-material structure correlation to predict the reliability of < 5 μm diameter vias.

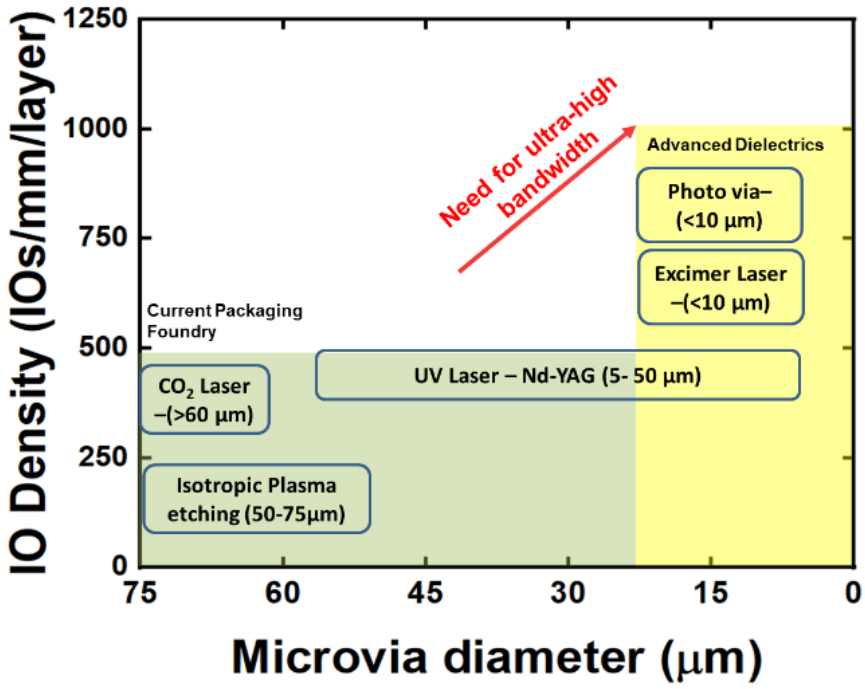


Figure 42 Strategic need for reducing microvia diameter to increase IO density

Previous studies have shown the influence of the mechanical properties of the polymer towards microvia reliability [31, 76, 77]. There has been effort in building a prediction model for different design parameters such as material, defect location and geometry [30]. However, all these studies are for > 20 μm via diameter. The reliability of sub 5 μm diameters and the influence of polymer material properties has not been studied.

Common failure mechanisms include via cracking induced by fatigue of the copper structure. This manifests as delamination at the interface between the via and pad [78, 79]. This can be influenced by the polymer material around the copper inducing thermomechanical stresses during processing. Further, the quality of plating also influences the formation of voids or other defects within the via which can affect microvia fatigue failure [77, 80].

In this study, we have looked at the effect of a) geometry and b) material properties on copper fatigue in microvias. The focus is on fully filled sub 5 μm diameters. A regression model was built to quantify the influence of different factors. Further, a daisy-chain test vehicle was design for thermal cycling and the experimental reliability results of 3 μm diameter microvias is reported. The findings of this paper will provide guidance on materials and geometry design for manufacturing reliable <5 μm diameter microvias.

5.1.1.2 Thermo-mechanical modeling of microvias

Finite-Element-Modeling (FEM) was performed using ANSYS Workbench to simulate the thermomechanical stresses and strains in the RDL structure. The geometry was built using Solidworks. Microvias in RDL consist of two different materials with varying coefficients of thermal expansion (CTE) bonded together. The modulus of the material also plays a significant role in determining the stresses induced. The geometry of the microvia is a key parameter in changing the overall strains. These microvias are formed using ablation processes and go through a thermal regime of extended times at high temperature during fabrication (copper plating and annealing, dielectric curing). Accelerated testing that involves thermal cycling the test-structure between extreme temperatures is used to study the reliability of these microvias and is part of qualification to simulate the real time loading that they will undergo.

5.1.1.2.1 Geometry:

The key structural design parameters studied in this work are via diameter and aspect ratio as shown in Figure 43 (a). The via diameter values used were 2 μm, 3 μm and 5 μm. The aspect ratio parameters were 1.0 and 1.67. The aspect ratio is calculated as the height of the via divided by the via diameter, which implies that for an aspect ratio of 1.67 and via diameter of 3 μm, the height of the via is 5 μm. The top pad and the bottom capture pad are maintained constant at 10 μm diameter and 5 μm height. The taper angle used here is 10^{o}. The control of the taper angle is usually limited by the via formation technique and

can be controlled in the range of 10^{o} – 30^{o}. The pad diameter is influenced by the lithographic tooling and is limited by the dimensional stability of the core substrate. The aspect ratio of the microvia becomes a critical parameter because of the trend of moving towards thinner dielectrics for electrical performance [81]. The material properties of interest are of the polymer material and the copper. Fully-filled electrodeposited copper has a standard set of material properties [82], while the polymer material used can be varied. Hence, the co-efficient of thermal expansion (CTE) and Young's modulus (Y) of the polymer material were varied in this study. The chosen parameters were 30 ppm/^{o}C, 45 ppm/^{o}C and 60 ppm/^{o}C for the CTE and 1.5 GPa, 3 GPa and 7.5 GPa for the Young's modulus. These properties were chosen after studying PID candidates (BCB, fluropolymer, phenolic resin, epoxy) or non-PID epoxy dielectrics with nano-sized fillers that are capable of supporting <5 μm diameter vias.

The 3-D model of the microvia built is as shown in Figure 43 (b). Due to the symmetry of the structure, each via model is $1/4^{th}$ of the actual microvia. The sides of the via were constrained to account for symmetry and periodicity of the via. The bottom of the microvia was constrained to take into account the effect of the substrate.

This study was carried out as a full-factorial DoE for 4 factors and resulted in 54 experiments (6 geometry X 9 material sets). In order to maintain consistency, the size was the mesh was maintained across all 6 geometries.

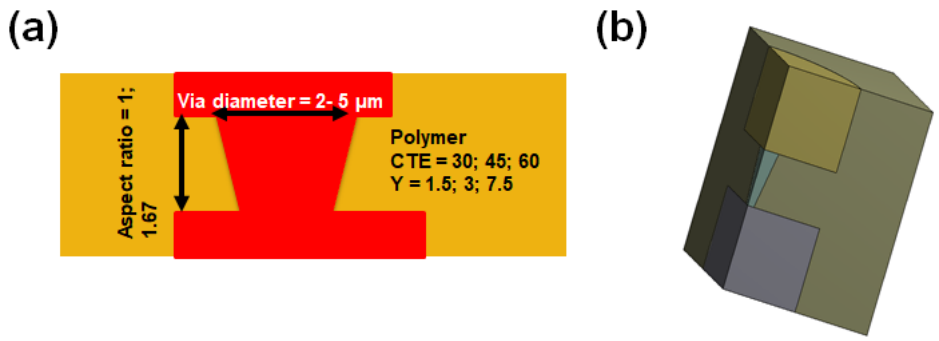


Figure 43 (a) Schematic cross-sectional drawing of modeling microvia with the key parameters as polymer CTE and modulus, aspect ratio and via diameter (b) 3-D model of 1/8th of microvia

5.1.1.2.2 Material Models and evaluation parameter

The material properties used in the simulation are given in Table 9 and have been used previously by [83, 84]. All materials are assumed to be isotropic. A bilinear kinematic hardening model was used for copper with a yield strength of 172.3 MPa and tangent modulus of 1034 MPa. The glass transition temperature of copper was chosen as 108 ºC based on [85]. The polymer was modeled as linear elastic with a glass transition temperature as 180 ºC to be representative of ultra-low k dielectric materials [81]. Since the thermal loading was below the glass transition temperature of the dielectric materials, the creep of the dielectric materials is negligible. Effect of a very thin Ti adhesion layer is neglected. Figure 44 shows the thermo-mechanical loading applied to the microvia. The modeled structure mimicked MSL-3 preconditioning followed by JEDC22 – A104B thermal cycling. The ramp and hold times are sufficient to allow full convergence of the model. Each time step was broken into a maximum of 100 sub time steps. Considering that both material models are rate-independent the effect of creep was not considered. During thermal cycling, the difference in material properties between the electrodeposited copper and polymer creates strains in the copper. The total strain range in the copper per thermal cycle is an important parameter for determining the low-cycle fatigue life of the microvia. The total strain range is the summation of the elastic and plastic strain range. The mirovias in this study were subjected to five thermal

cycling steps to achieve steady state conditions with less than 2% variation and the accumulated strain difference between the last two cycles is taken as the total strain range.

Table 10 Material properties used in mechanical modeling

Material	Model
Copper	• Bilinear kinematic hardening model • Modulus: 117 GPa • CTE: 17 ppm/C • Poisson's ratio: 0.33 • Yield stress: 172.38 MPa • Tangent modulus:1034.2 MPa • Stress-free temperature = 108 °C
Polymer	• Elastic with temperature dependent CTE (30 – 60 ppm/°C) and Young's modulus (1.5 – 7.5 GPa) • T_g = 180 °C

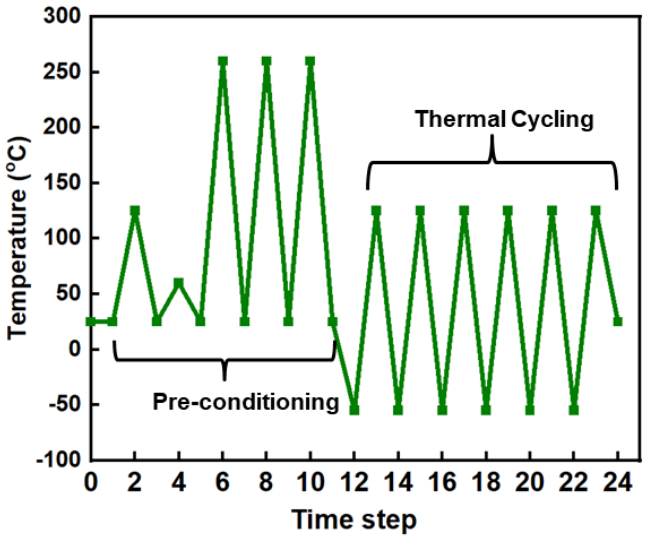


Figure 44 Thermomechanical loading on the structure to simulate thermal cycling test.

5.1.1.2.3 Physics of failure models for electrodeposited copper fatigue life

The cycles to failure for a given value of the total strain calculated through the models is determined using empirical models. The total strain range consists of the elastic and plastic strains:

$$\Delta\varepsilon = \Delta\varepsilon_{el} + \Delta\varepsilon_{pl} \quad (3)$$

Where $\Delta\varepsilon$ is the total strain range, and $\Delta\varepsilon_{el}$ and $\Delta\varepsilon_{pl}$ indicate elastic and plastic strains respectively. Th combined Basquin and Coffin-Manson fatigue equation [86, 87] approximates it as:

$$\Delta\varepsilon = \frac{\sigma_f'}{E}(2N_f)^b + \varepsilon_f'(2N_f)^c \quad (4)$$

$$\Delta\varepsilon = N_f^{-0.6}D_f^{0.75} + 0.9\frac{S_u}{E_{cu}}\left(\frac{e^{D_f}}{0.36}\right)^{0.1785log\frac{10^5}{N_f}} \quad (5)$$

Where, the $\frac{\sigma_f'}{E}$ = 0.00741, b=-0.11, ε_f' = 0.709 and c=-0.6 and N_f is the total cycles of failure. The Engelmaier model [88] is also used to estimate the total strain and is given by:

Where, D_f = 0.302, S_u=400 MPa and S_u/E_{cu} = 0.0034188 and N_f is the total cycles to failure. These properties have been assumed for electrodeposited copper and for a total resistance change of 20% in the daisy chain structure. These material properties have been widely used to predict microvia fatigue life [30, 75, 89, 90].

5.1.1.2.4 Effect of Geometry

The effect of changing the geometry is summarized in Figure 45. The two parameters studied were the via diameter and aspect ratio.

As shown in Figure 45 (a) as the via diameter decreases the total strain range (TSR) increases. There are two key inferences from this analysis a) the slope of the lines indicates that the CTE has a stronger effect on large via diameters than smaller via diameters b) reducing the via diameter reduces the tolerance for material properties, which means that for a 2 μm diameter a lower CTE dielectric is required to ensure TCT reliability.

Figure 45 (b) shows the effect of aspect ratio on the TSR. From this analysis, it can be seen that a lower aspect ratio is favorable for a 5 μm diameter which aligns with previous studies [31]. However, on reducing the via diameter down to 2 μm the trend inverts and we see that a higher aspect ratio is more favorable and shows lower TSR. It is hypothesized that a higher aspect ratio of 1.67 in a 2 μm diameter via only increases the overall height of the via by 1.34 μm compared to an increase of 3.35 μm for a 5 μm diameter via. It is hypothesized that this small increase does not warrant a strong effect on the microvia reliability and the microvia is aided by the increased polymer volume in stress relaxation. Hence, we conclude that an aspect ratio of 1.67 is not very different from 1 for a 2 μm diameter via. Further, the lower CTE dielectrics show a greater effect on the TSR as seen in the difference in TSR values for a 30 ppm/^{o}C dielectric compared to a 60 ppm/^{o}C dielectric in a 5 μm diameter via.

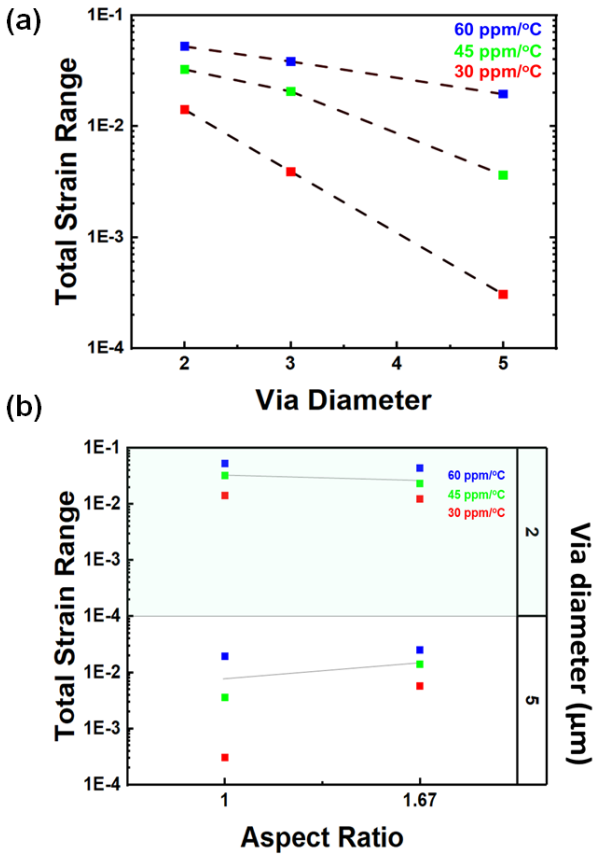


Figure 45 (a) The variation in total strain range as a function of via diameter (log-linear). The aspect ratio is 1 and young's modulus of 1.5 GPa. (b) The variation in total strain range as a function of aspect ratio (log-linear); The two-halves of the figure are for different via diameter with the top half depicting 2 µm via diameters and the bottom half depicting 5 µm via diameters; The line connects the average of an aspect ratio of 1 to 1.67 for all CTEs; The young's modulus is 1.5 GPa. The colors indicate different CTE's of the polymer material, with red being 30 ppm/°C, green being 45 ppm/°C and blue as 60 ppm/°C.

5.1.1.2.5 Effect of polymer dielectric material properties on copper strains

The effect of changing material properties is shown in Figure 46. The two parameters studied are co-efficient of thermal expansion (CTE) and young's modulus. As shown in Figure 46 (a), as the CTE increases the TSR increases. Increasing the CTE of the polymer increases the CTE mismatch between the copper and polymer, thereby increasing the TSR. As seen in Figure 46 (b), as the young's modulus increases the TSR increases. This can be interpreted as the polymer exerting more stress on the copper as

it becomes stiffer. From this we understand that for a reliable microvia design for 2 µm diameter, it is required that the polymer material have low CTE and modulus, while a 5 µm diameter has a greater tolerance range for polymer material properties.

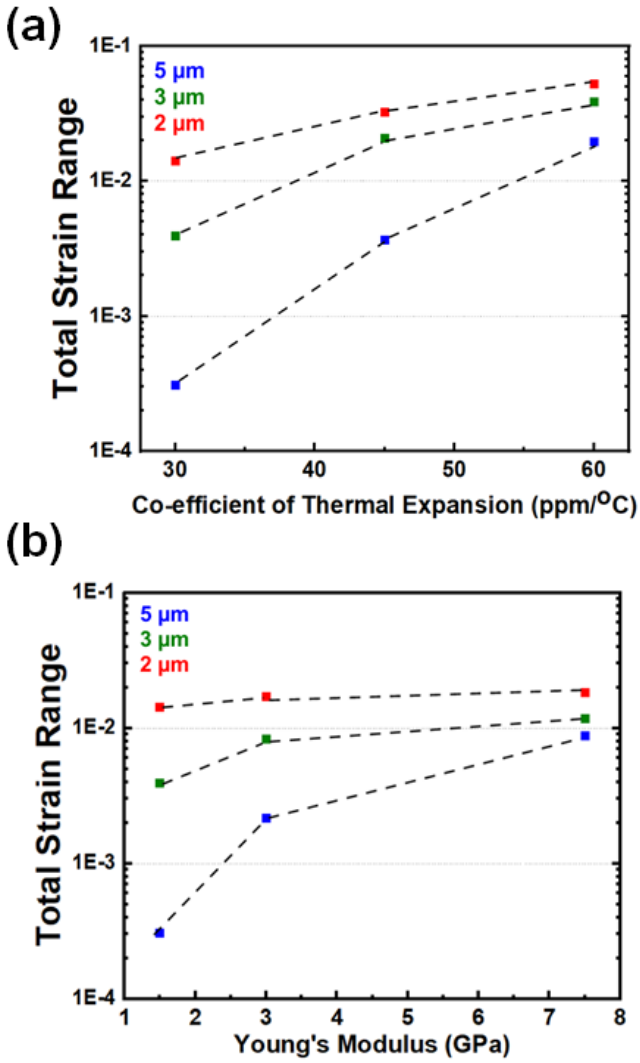


Figure 46 (a) The variation in total strain range as a function of the polymer co-efficient of thermal expansion (CTE) (log-linear). The aspect ratio is 1 and Young's modulus is 1.5 GPa. (b) The variation in total strain range as a function of the polymer young's modulus (log-linear). The aspect ratio is 1 and CTE is 30 ppm/°C. The colors indicate different via diameters with red being 2 µm, green being 3 µm and blue being 5 µm.

5.1.1.2.6 Regression Model

To understand the effect of all 4 factors, a first-order strain-life based regression model was developed. A statistical software based on the R package was used to perform this analysis [91]. The full-factorial DoE was based on four parameters – via diameter with three levels, aspect ratio with two levels, CTE with three levels and young's modulus with three levels and resulted in 54 experiments that formed the dataset. The entire dataset is given in the appendix in Table 13. The independent variable was the TSR/1000. All parameters expect for aspect ratio were modeled as dependent numeric variables. The aspect ratio was modeled as a dependent factor. The regression coefficients are given in Table 10 and they are the estimates of the parameter. For example, the coefficient of the CTE can be interpreted as for every 1 ppm/^{o}C increase in the CTE the TSR/1000 will increase by an average of 0.975 all else being the same. All estimates expect for the aspect ratio are statistically significant in the 95% confidence interval. This is hypothesized as being because of the shift from negative to positive influence of the aspect ratio as seen in Figure 45 (b). The estimates indicate that the greatest influence on the TSR is from the via diameter with a co-efficient of -4.370. In comparing the coefficients of the CTE (0.975) and young's modulus (1.204), we can see that an increase of 1 unit for the young's modulus has a greater influence on the TSR than the CTE.

The assumptions of the multiple linear regression such as the normality of the residuals, homoscedasticity, lack of autocorrelation and lack of multicollinearity were verified. The predicted strains from the regression model agree well with the actual strains as is seen in Figure 47 with a R-squared value of 0.924.

Table 11 Coefficients of regression model

	Co-efficient	Std.error	p.value
Intercept	-9.276	2.76	0.002
CTE	0.975	0.04	<0.001
Y	1.204	0.21	<0.001
Diameter	-4.370	0.44	<0.001
AR|1.67	-1.210	1.10	0.278

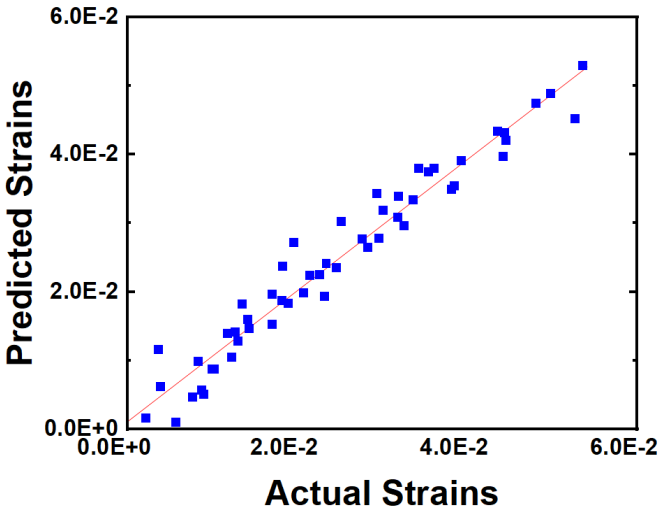


Figure 47 Relationship between strains predicted by the regression equation (predicted strains) and the strains determined by the FEM model (actual strains)

From Figure 48 the combined influence of all parameters on the TSR can be understood. Figure 48 (a) which shows the influence of aspect ratio on TSR is confounded by the influence of the microvia diameter and shows a slight negative influence of higher aspect ratio of TSR. Figure 48 (b) shows an increase in the average strains as the CTE increases. Figure 48 (c) shows a decrease in strains as the via diameter increase. Figure 48 (d) shows an increase in strains as the young's modulus increases. These trends on the overall dataset match the observations in the earlier sections.

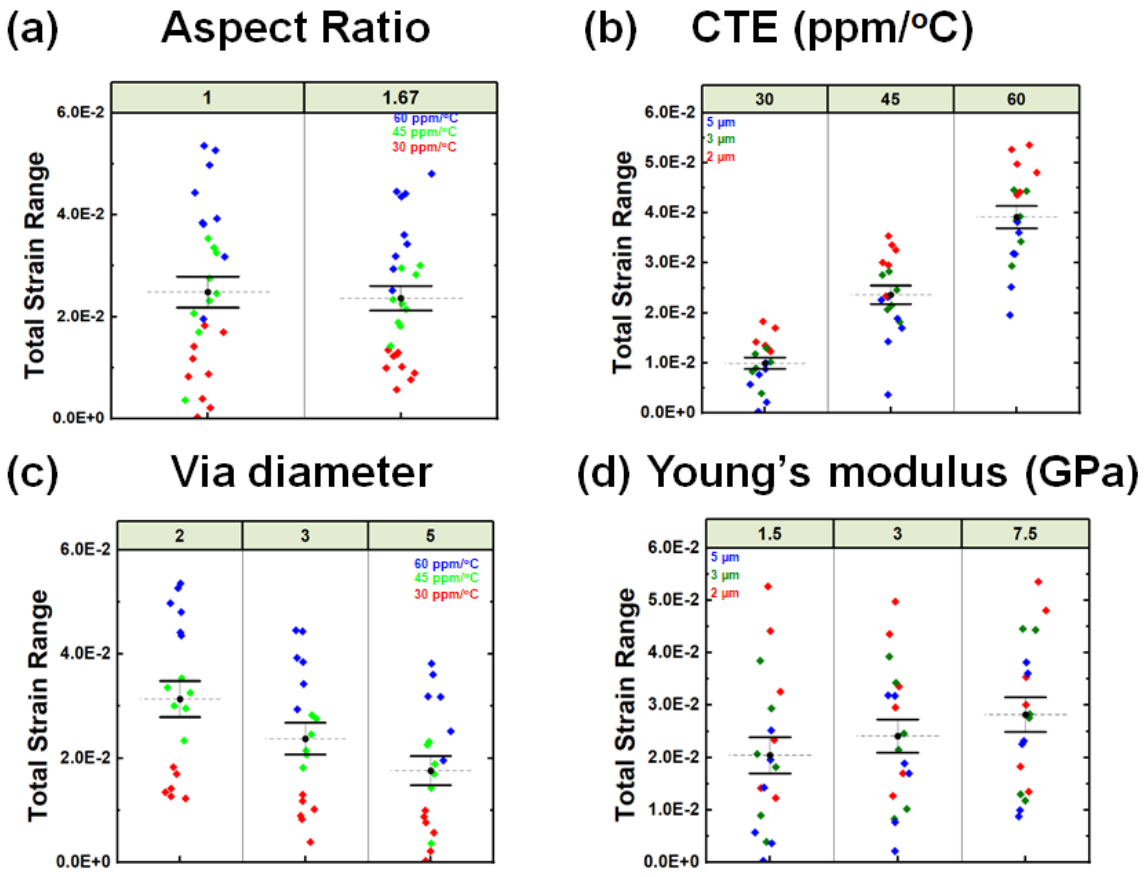


Figure 48 TSR versus (a) aspect ratio (b) CTE (c) via diameter (d) young's modulus. The color coding on (a) and (c) is to indicate different CTE's of the polymer material, with red being 30 ppm/°C, green being 45 ppm/°C and blue as 60 ppm/°C. The color coding on (b) and (d) indicate different via diameters with red being 2 µm, green being 3 µm and blue being 5 µm.

5.1.1.2.7 Effect of via pitch

To capture the effect of neighboring microvias, a 3D model was built according to the unit cell shown in Figure 49 (a) and (b). Only four nearest neighbors were considered for this study. The via pitch is defined as the center to center distance between two microvias and it was varied from 20-40 µm. As is seen in Figure 49 (c) increasing the via pitch reduces the total strain range. This can be interpreted as there being a stronger effect of the neighboring vias at reduced pitch. This study was performed for a worst-case scenario of a 60 ppm/ºC CTE and 7.5 GPa modulus.

5.1.1.3 Fabrication of sub 5 µm diameter microvias

In this work, the reliability of sub 5 µm diameter vias fabricated using a novel photosensitive material has been studied. Here, we used a dry-film based photo-imageable dielectric (PID) with an underlying epoxy and carboxylic acid resin mix. The material properties of the PID are given in Table 11. For the purpose of thermal cycling test, a daisy chain test-structure as shown in Figure 51 (a) and the process flow is given in Figure 50. The PID was laminated on a 6" glass panel using a vacuum laminator. An exposure dose of 200 mJ/cm^2 on an i-line 365 nm wavelength tool was used to pattern the PID followed by development. Then, the PID was exposed to 2 J/cm^2 of UV light with broad spectrum followed by a thermal treatment at 180 ºC for 60 mins to fully cure the dielectric. A semi-additive process is used to pattern the dielectric and this process is detailed elsewhere [81, 92]. Figure 51 (b) shows the fabricated test-structures used for the thermal cycling test. An average of 400 microvias were fabricated per test coupon.

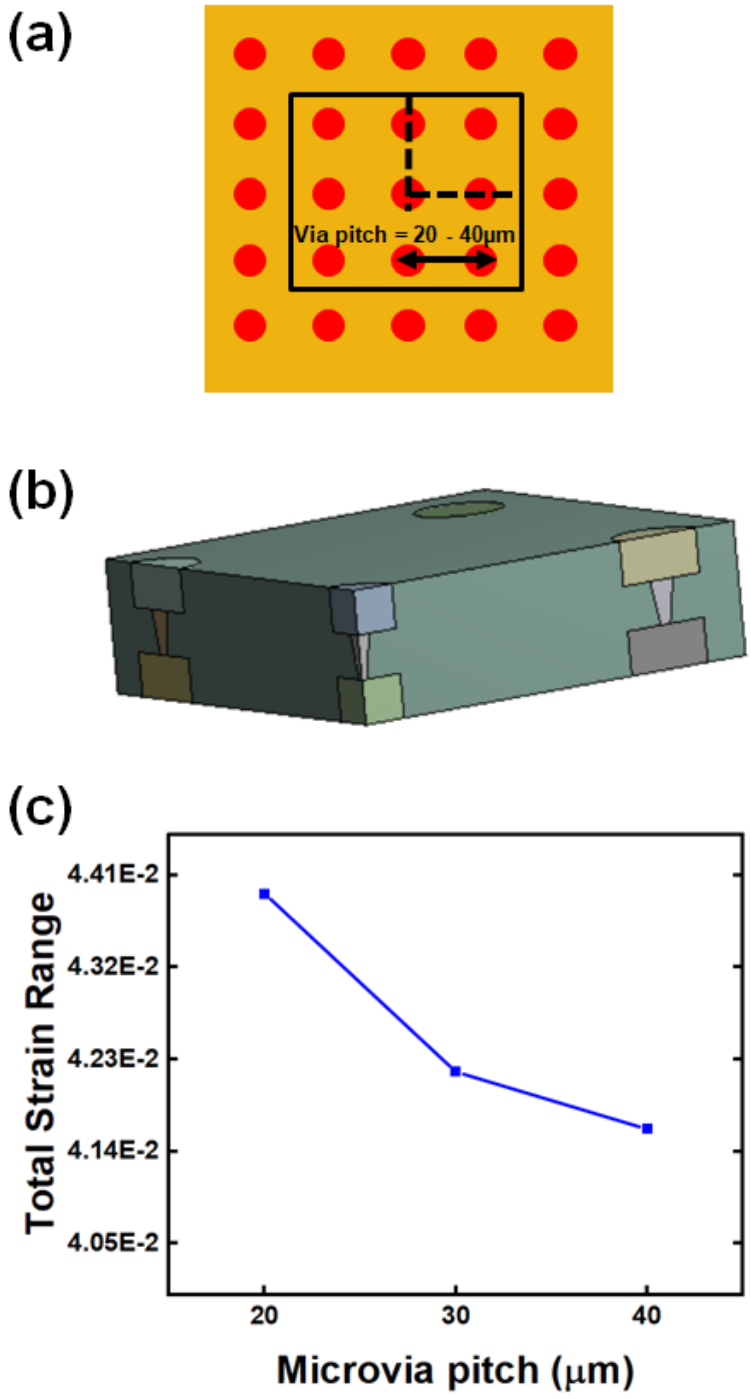


Figure 49 (a) Representative unit cell used for modeling (b) 3-D model of 1/8th microvia (c) Total strain range versus microvia pitch. The via diameter is 3 µm, aspect ratio = 1.67, CTE = 60 ppm/^{o}C, and young's modulus of 7.5 GP

Table 12 Material Properties of the photo-imageable dielectric

Property	**Value**
T_g	180-185 ºC
CTE	30-35 ppm/ºC
Y	3.5-4.0 GPa
Tensile strength	90-95 MPa
Elongation	5.5-6.0 %
D_k	3.3
D_f	0.019
Water absorption	0.84%

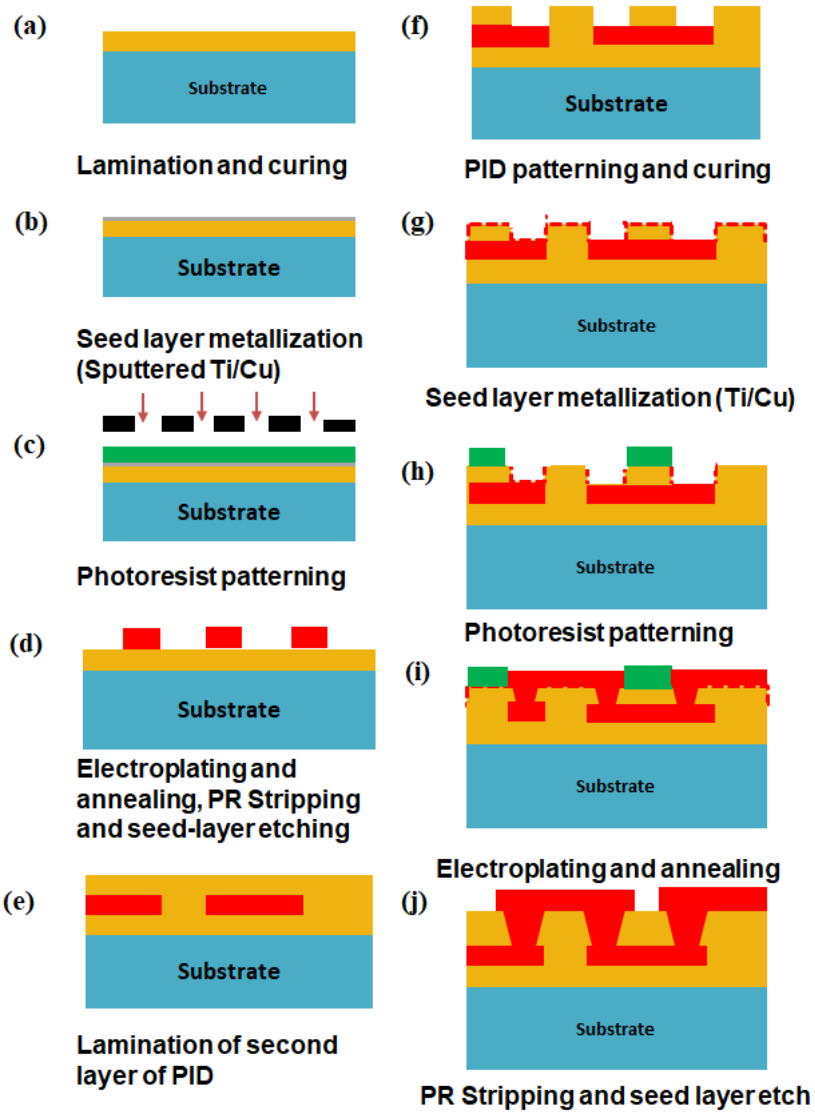


Figure 50 Process flow for fabricating daisy-chain test structures

Preconditioning was carried out according to MSL-3 requirements. The test-structures were dried at 125 ºC for 23 hours. After drying, the sample was places in a humidity chamber at 60 ºC, 60 % RH for 120 hours. Thermal cycling was conducted following JEDEC JESD22-A104D standards, between temperatures of -55 ºC and 125 ºC with a dwell time of 15 mins at each temperature, completing one cycle/hour. The resistance was measured every 100 cycles using a four-terminal method and a failure

criterion of 20% resistance change was used. From Figure 52 we can see that at ~1700 cycles the resistance change is >20%.

The finite-element model developed was used to predict the number of cycles to failure using the empirical equations. The TSR was estimated to be 8.97E-03 and as we see from Table 12, the coffin-manson;basquin model predicts it to be 1470 cycles and the engelmaier model predicts it to be 1930 cycles. The experimentally calculated failure point at 1700 cycles falls between the two models which indicates that the finite-element model has good correlation with the experimental data.

Failure analysis of the daisy-chain test structure was carried out by measuring the resistance of a 20 via row after thermal cycling test. Approximately 15% of the vias showed very high resistance. Focused ion beam (FIB) was used to image the microvias and study the failure mode. A thin hairline crack is seen at the via/pad interface as in Figure 53 (b). The 6 vias in the 20 via row were imaged and the same failure mode was observed. This crack is because of the difference in material properties of the polymer and copper. Although the pad and microvia are both fully filled with electroplated copper, there is a discontinuity at the interface because they were fabricated at different time steps and do not form a homogeneous interface. This interface is the weakest link in the entire daisy chain and cracks when the stress increases beyond the critical G_c.

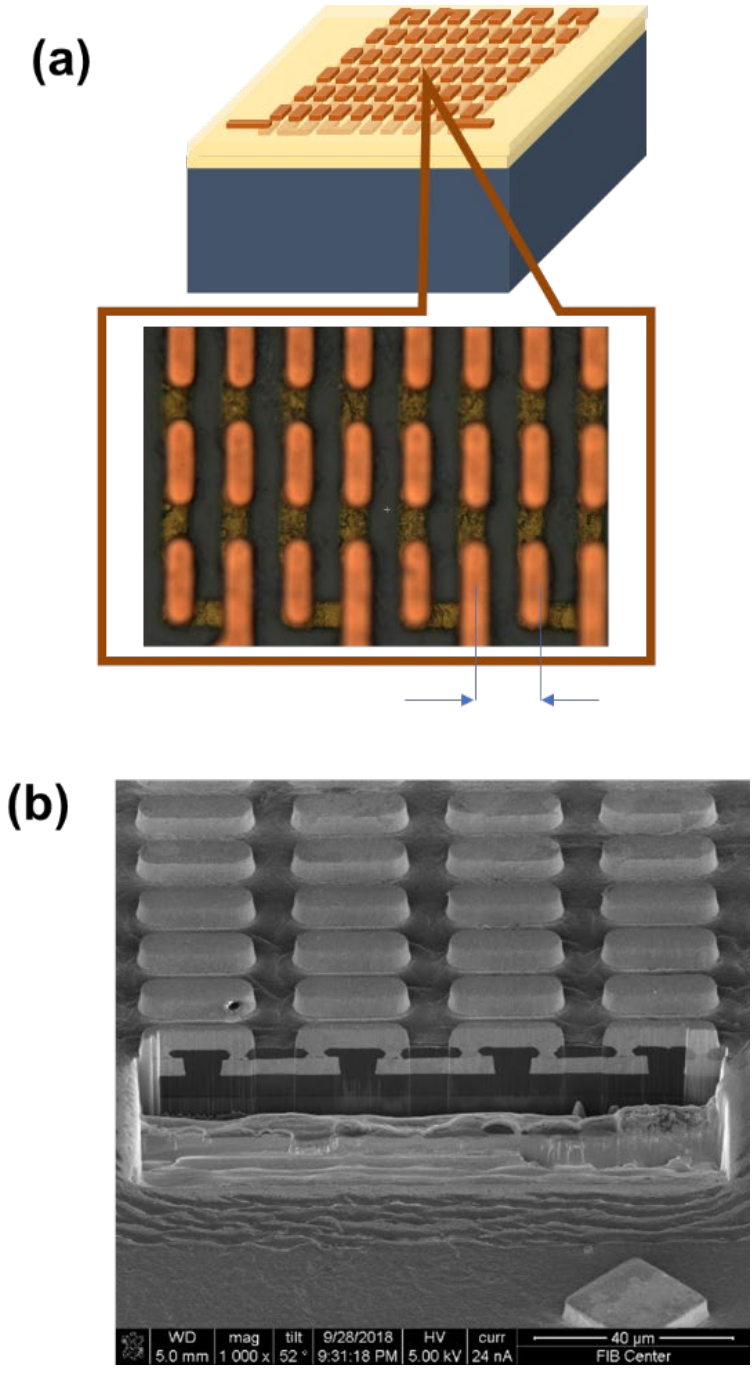


Figure 51 (a) Daisy chain structure for TCT testing. A total of 400 vias were tested in a 20X20 via pattern (b) SEM cross-section of the daisy-chain structure of 3-5 µm diameter microvias.

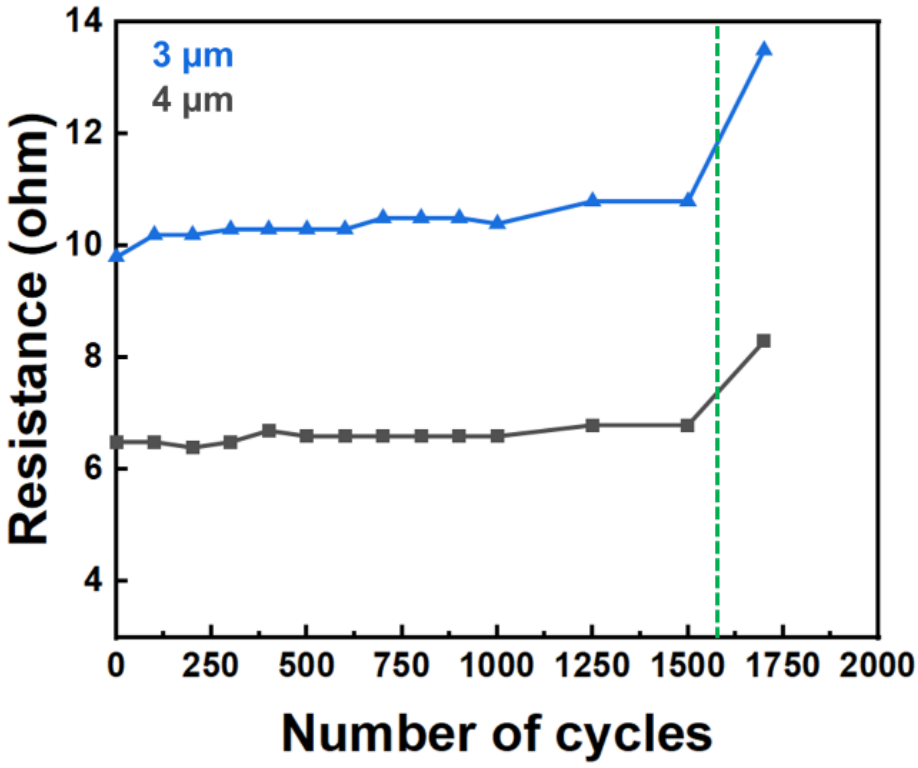


Figure 52 Resistance of the daisy-chain structure versus the number of TCT cycles. The color coding indicates different via diameter, blue is 3 µm and grey is 4 µm.

Table 13 Fatigue-life calculations; Correlating modeling predictions with experimental data for 3 µm diameter vias

Property	**Number of cycles**
Experimental	1700
Coffin-Manson; Basquin	1470
Engelmaier	1930

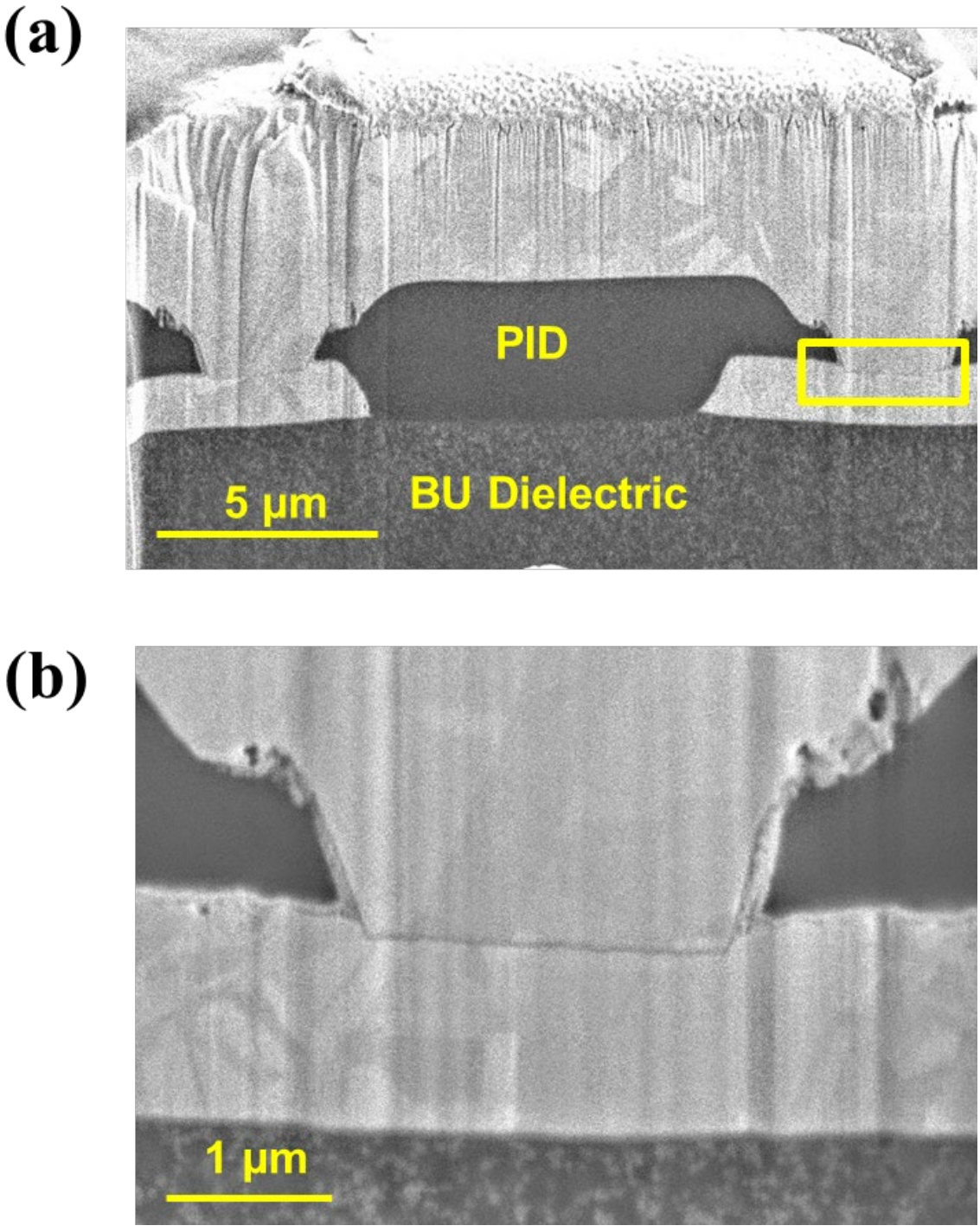


Figure 53 FIB cross-section SEM of daisy-chain test coupons after thermal cycling. (a) representative unit structure; the rectangle indicates the failure location (b) single 3 µm diameter microvia

5.1.1.4 Summary

This study presents finite-element modeling, panel-scalable fabrication processes and reliability characterization for ultra-fine pitch <5 μm diameter microvias. Thermo-mechanical modeling results indicate that in order to lower the microvia diameter, controlling the polymer dielectric CTE and young's modulus is critical. During TCT, all samples passed JEDEC-based thermal cycles. Failures were recorded at above 1700 cycles. Experimental results indicate excellent correlation with the thermomechanical modeling predictions. Thus, this study provides a fundamental insight into the effect of geometry and material properties on the reliability of <5 μm diameter microvias.

5.1.2 Single-layer thermo-mechanical reliability

This section explores the stress than builds up in the fabrication of a single RDL layer due to the difference in polymer and copper material properties during the high-temperature processing steps.

5.1.2.1 Background and overview

The stresses that build up in a substrate can lead to package failures such as delamination, popcorning or warpage [40, 93, 94]. The mechanical properties of the polymer have an important influence in determining the thermo-mechanical stresses of the re-distribution layer (RDL). There are two types of stresses that are inherent to the RDL stack-up a) intrinsic stresses b) thermal stresses. Intrinsic stresses result from the deposition and curing processes of the polymer and depend on the polymer chemical structure and rheology. The thermal stresses are induced by the difference in mechanical properties between the copper and build-up dielectric. The coefficient of thermal expansion (CTE) and the young's modulus mismatch between the two materials induce stresses when the RDL is taken to elevated temperatures and cooled down. These stresses can be compressive or tensile in nature. Tensile stresses

lead to cracking at the interface while compressive stresses can prevent the emergence of cracks at the interface but can also lead to blistering of the film. In previous works, there has been a study of the influence of metal deposition on stress on a wafer [36], of stress management during polymer deposition and curing [34] and on influence of RDL stress on warpage [95]. However, a process study on the impact of how the fabrication of RDL influences the stress build up in the wiring layers has not been done. This study looks at the stress induced in the polymer RDL layers because of the semi-additive fabrication process.

5.1.2.2 Fabrication of test-structures

The material properties of the dielectrics used for this study are given in Figure 54 (a). These test-structures were fabricated using a semi-additive process (SAP). Silicon wafers of 1 mm thickness with low TTV is used in this work. The process flow involves lamination of the dielectric using the Meiki vacuum laminator with 90 s of pulling vacuum and 60 s of pressure of 0.5 MPa at 90 F. The polymer was cured at the recommended cure temperatures for >90% crosslinking. Material B has a higher cure temperature than material A. Seed layer metallization was done by sputtering 50nm Ti/ 150nm Cu using a Denton RF/DC sputter tool. The test-structures were annealed following this at 150 ºC for 30 minutes. This is followed by electroplating using a commercial plating bath from Atotech Cupracid^{TM} to a thickness of 5 – 7 µm. Finally, the sample was annealed at 190 ºC for 30 minutes to fabricate one RDL layer. The same process steps are repeated to fabricate consecutive RDL layers. The residual stress was determined using the bowoptic optical wafer stress measurement. The residual stress of the polymer RDL layers was measured using the wafer curvature with the Stoney equation as given below:

$$\sigma_f = \frac{E_s t_s^2}{(1-\upsilon)6rt_f} \tag{6}$$

Where t_s is the substrate thickness, t_f is the film thickness and υ is the poisson's ratio of the [96]. The radius of curvature was measured using the bow of the wafer. Depending on the direction of bow, the stress can either be compressive or tensile as shown in Figure 54 (b). The wafer curvature method assumes that the film is very thin compared to the substrate and that the deformations are very small. Two samples were fabricated and a total of 3 measurements per sample were made with <5% error.

(a)

	Material A	Material B
Elongation to failure	5.6%	13%
CTE	39 ppm/K	63 ppm/K
Young's modulus	5 GPa	2.9 GPa
Film-type	Dry-film	Dry-film
Thickness	15 µm	19 µm
Polymer	Epoxy	BCB

(b)

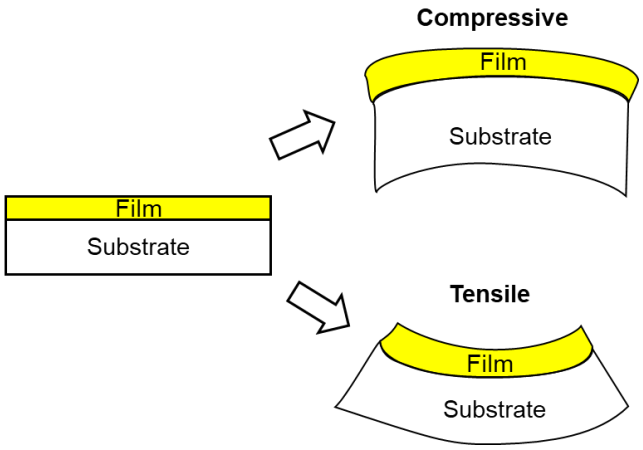


Figure 54 (a) Material properties of dielectric (b) Schematic of effect of thin-film stress on substrate

5.1.2.3 Residual Stress

The residual stress for sequential processing steps is shown in Figure 55. The initial stress state of the polymer dielectric after lamination and cure is based on the polymer structure and degree of crosslinking. This can be further optimized by managing the cure process and reducing the temperature of the cure for thermosets. The stress can also be changed by cure method used such as microwave or UV cure. The difference in the stress states persists through the processing steps and shows the importance of maintaining a low residual stress state after cure. From Figure 55 we see that the stress changes significantly during the annealing steps. The effect of the copper plating comes in after annealing and a maximum RDL stress of ~90 MPa is reached. Further, the stress development during processing the second layer follows a similar trend to the first layer and increases during annealing cycles. The second layer stresses do not increase beyond the first layer. This is because the thickness of the film increases along with the radius of curvature, thereby reducing the overall increase in stress as given by stoney's equation. The maximum stress usually seen after annealing the first copper layer is dependent on the coefficient of thermal expansion (CTE) and modulus mismatch between the copper and polymer. A higher CTE material such as material A with a CTE of 63 ppm/^{o}C shows a higher stress than material B with a CTE of 39 ppm/^{o}C. These findings show that low CTE and low modulus materials are favorable and that the initial residual stress can be a useful predictor of how stress develops through the processing steps. The overall stress in the package is dependent on the substrate core and from this study we see that balancing the RDL stress using a double side process is critical, particularly in ultra-thin packages

5.1.2.4 Summary

This work looks at the stresses developed in the RDL layers during processing and studies the impact of polymer properties on the residual stress. Low-CTE, low-modulus materials show much lower stresses

compared to high-CTE materials. These stresses increase when the structure passes through high-temperature processing but is much lower than high-CTE materials.

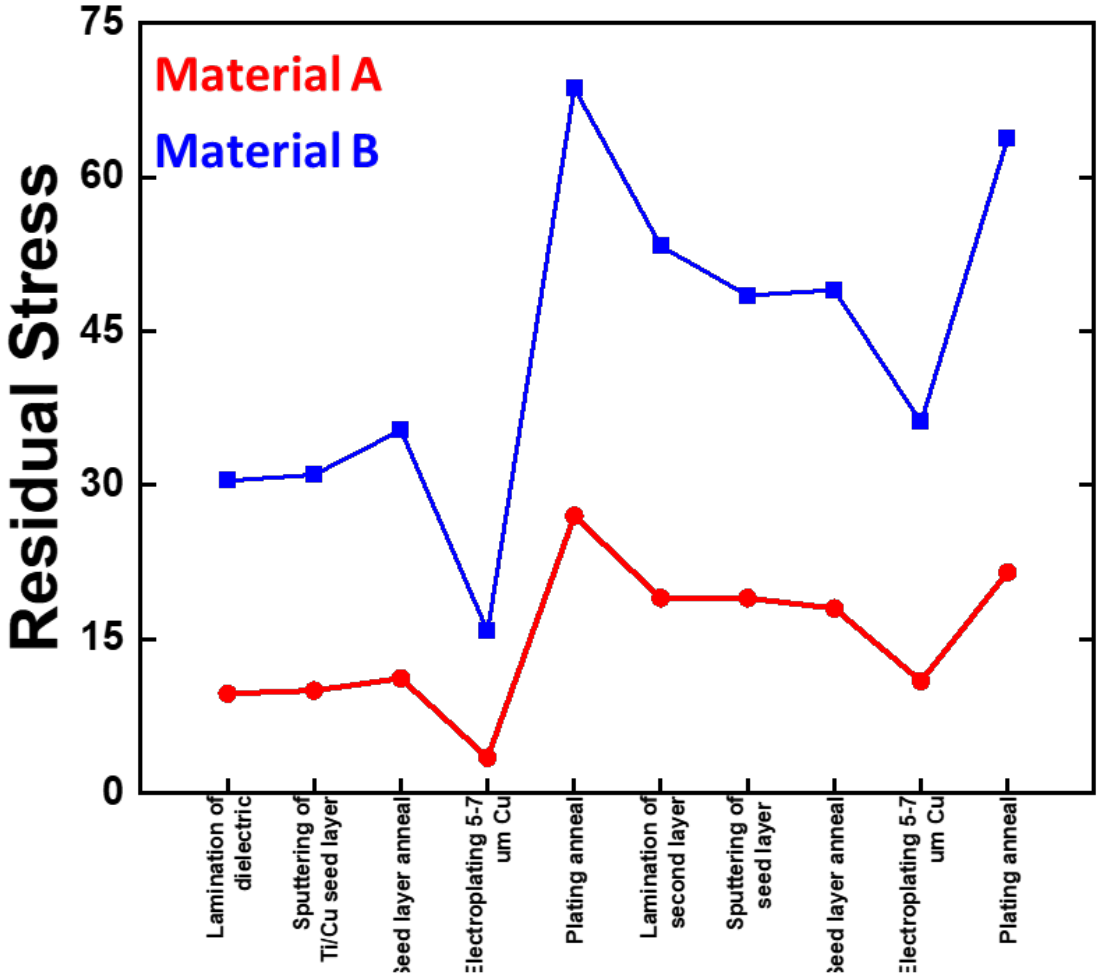


Figure 55 Compressive stresses on the polymer RDL layers. The different process steps represent the polymer deposition and metallization steps involved.

5.2 Chemical reliability – polymer/copper interfacial adhesion

Metal-polymer adhesion is particularly important for microelectronics packaging where the demand for higher bandwidth systems requires higher interconnect density. Typical packaging architectures are

comprised of multiple metal-polymer interfaces. These interfaces are prone to several failure modes, including interfacial delamination, cohesive cracking, and warpage [40, 41]. Interfacial reliability is becoming a major concern in advanced polymer substrates used in redistribution layers (RDLs) for two reasons: (1) polymer dielectrics are shifting towards more inert chemistries, driven by the need for higher signal speed which is enabled by low dielectric constant polymers with non-polar bond groups and (2) the need to operate packages at higher powers and higher temperatures, driven by mega trends in power and automotive electronics [42]. Traditional epoxy-based RDLs contain highly polar functional groups which adhere well to metal thin-films but are challenged by higher dielectric permittivity and substantially higher RC signal delays. Advanced low-dielectric constant polymeric resins that are stable at higher temperatures are sought for next-generation polymer dielectrics. Examples of such emerging dielectrics are benzocyclobutene (BCB), polyimide (PI) and fluoropolymer-based resins [29]. The chemical nature of these polymers is such that they do not bond to a sputtered adhesion layer or cannot be metallized easily using electroless copper. Further, the weak interfaces can become a site for moisture condensation, increasing the potential for delamination. Under aggressive temperature and humidity stress tests, interfacial delamination is a critical concern because of the poor adhesion strength of the polymer to the metal. These temperature requirements become more apparent for packaging of wide bandgap power electronics devices, like those based on Gallium Nitride (GaN) or Silicon carbide (SiC) [97].

Several approaches exist for enhancing metal-polymer adhesion. The polymer surface can be oxidized via plasma or chemical treatments to promote bonding to a reactive metal (e.g, chromium) [43]. The polymer surface can be roughened to create mechanical anchoring sites that increase adhesion[98, 99]. Coupling agents can also be added to the polymer to create reactive sites to which the metal layer can bond [100]. Here, we explore the use of a process known as vapor phase infiltration (VPI) [101-104] or sequential infiltration synthesis (SIS) [105-114] to infuse inorganics into the subsurface of the polymer

and increase adhesion. VPI is a gas phase processing technique that exposes polymers to metalorganic vapors that sorb, diffuse, and become entrapped within the bulk (subsurface) of the polymer [104]. In some ways, this process is a combination of all three adhesion promotion methods cited above; the infiltrated inorganic serves to increase chemical bonding across the interface, it creates mechanical interlocking within the polymer bulk, and it is essentially a post-process additive to the polymer chemistry.

5.2.1 Technical Approach

Hybrid inorganic-organic materials have been used to tune the properties of materials to create favorable surface characteristics [115]. There are different ways in which these hybrid materials are created, and the control of the properties of the final material can be achieved by controlling the size and morphology of these domains of inorganic/organic interactions. Sol-gel and chemical vapor deposition (CVD) techniques have been explored to create hybrid materials with tailorable properties [116]. Atomic Layer Deposition (ALD) has been used to create conformal defect-free inorganic coatings on polymers and other organic surfaces [117]. A subsurface interaction of the precursor used in ALD with the polymer can dramatically alter the surface characteristics of the soft material and can be used to create hybrid interfaces. This technique called vapor-phase-infiltration [104] can be used to control the depth and density of the inorganic infiltration into the organic substrate thereby tailoring the hybrid material properties. VPI has been used by researchers to enhance the mechanical properties of spider dragline skills [105, 118] improve the etch properties of photoresist [105], and increase in the tensile strength of PTFE which showed that VPI could modify synthetic polymers [119].

An innovative vapor-phase-infiltration (VPI) approach is demonstrated to modify the subsurface of polymer dielectrics and tailor interfacial properties between the re-distribution layer (RDL) build-up dielectric and metal. This approach can be used to tune the surface properties of the polymer and create

novel hybrid sub-surfaces with improved adhesion characteristics. The chemical and structural modification after VPI is discussed, followed by the adhesion performance improvements seen and finally, a brief hypothesis about potential reaction mechanisms is suggested for the performance improvement. We find that, there is a key range over which VPI parameters can be modified to maximize adhesion.

5.2.2 Test Structure

5.2.2.1 Materials Synthesis:

Dry-film rolls of a Benzocyclobutene-based polymer (dielectric constant (D_k) of 2.65 and a loss (D_f) of < 0.0008) were used as the exemplary RDL polymer dielectric. These polymer films were either 9 or 19 μm thick. While the exact polymer chemistry is proprietary, it is based upon Dow Chemical's CYCLOTENE 4000 series resin which is a Benzocyclobutene polymer with siloxane segments. It has a glass transition temperature of 300 °C and is a positive-tone photo definable polymer.

These polymer films were laminated to a low co-efficient of thermal expansion or CTE (3 ppm / °C) borosilicate glass (Corning). Prior to lamination, the glass panels were diced into 3'' squares and rinsed with solvents (acetone, isopropyl alcohol, and distilled (DI) water). An adhesion promoter (AP3000, Dow Chemicals) was spin-coated onto these glass substrates at 3000 rpm for 30s, followed by drying at 150 °C for 90s. A MEIKI MVLP300 vacuum laminator was used to laminate the dry-film polymer to the glass substrates. The lamination procedure required pulling vacuum for 90s and then hot-pressing at 0.6 MPa for 30 s at 93 °C. The polymer was then hard cured at 250 °C for 60 mins in a nitrogen atmosphere (99.9999% purity).

After curing, the polymer was vapor phase infiltrated in a custom-built, hot-walled reactor that exposed the polymer to a static atmosphere of metalorganic precursors. In this study, we specifically

focused on modification with trimethyl aluminum (TMA) at a pressure of ~1 Torr. The polymer dielectric was held in flowing ~1 Torr N_2 for 300 s prior to the process start. A single VPI sequence consisted of dosing TMA for 1 s / variable hold time in the TMA atmosphere / 1 s DI water dose / 90 s purge. Dosing sequencing was accomplished with custom designed LabView control software [120]. Polymers were VPI treated at temperatures ranging from 100 ºC to 175 ºC.

Plasma treatments of the polymer dielectric were conducted using a plasma them RIE (Plasma therm, Inc, 720). The pressure was maintained below 50 mtorr, a RF power of 250 W was used and Argon gas flow was 100 cm^3/min. The plasma time was varied between 5 and 20 minutes.

Metal films consisted of a thin (50 nm) sputter deposited chromium adhesion layer, a 200 nm sputter deposited copper layer, and a ~25 μm thick electroplated copper film. The initial layers were deposited via DC sputtering (Denton Discovery RF/DC Sputter tool, 40 sccm Ar, 100 W, 50nm for Cr and 200nm for Cu). Copper was electroplated under galvanostatic conditions using Atotech's Cupracid TP BKTM electrolyte solution, consisting of electropure Copper Sulfate solution, Sulfuric acid, Sodium Chloride, Cupracid TP Leveller, Cupracid Brightener and Cupracid starter. The copper film uniformity was maintained by keeping the ratio of organic to inorganic additives constant. Based on our experience, a plating rate (I/A) of 1 – 1.5 A/dm^2 is recommended to maintain copper uniformity.

Vapor phase infiltration processing sequence:

The infiltration process was carried out in a custom-built hot walled VPI reactor which is temperature-controlled using PID controllers. Valves are pneumatically actuated using compressed air. The first step in the infiltration process is purging with nitrogen, which is supplied at 250 sccm followed by pumping for a sufficient time to remove residual moisture. Then, the precursor (Trimethyl aluminum, 98%, Strem Chemicals, DANGER:pyrophoric) was dosed at a fixed process temperature to the chamber

for 1 s. The polymer material inside the chamber was exposed to the static precursor environment for various times. Next, room-temperature deionized water vapor was dosed for 1 s and exposed to the polymer material. The chamber was then purged down with nitrogen and evacuated to baseline. This process is termed as 1 cycle and is repeated for more cycles in certain cases.

5.2.2.2 Chemical and Structural Analysis:

Scanning electron microscopy (SEM, Hitachi SU8230), and energy dispersive X-ray (EDX) spectroscopy were used to probe morphological and chemical changes in the polymer material before and after VPI. To obtain good cross-sectional images, films were cryo-fractured by first dipping in liquid nitrogen and then fracturing via crack initiation with a diamond scribe. To minimized film damage and charging, SEM images were taken at an accelerating voltage of 1 kV. Water contact angle measurements (Rame-Hart model 250 Goniometer) were taken before and after infiltration to study changes in surface chemistry and wettability.

The depth profile of infiltrated polymer was measured with the time-of-flight secondary ion mass spectrometer (ToF-SIMS, IONTOF, 5 Series). SIMS spectra were collected using oxygen sputtering (150 μm X 150 μm) and bismuth analyzer beams (50 μm X 50 μm). Positive polarity was used to detect the Al+ signal from infiltrated TMA. The depth of the crater was measured using a KLA-Tencor P-15 profiler.

Fourier transform infrared (FTIR) spectrascopy was collected on a Thermo Scientific Nicolet IS50 spectrometer in the attenuated total reflectance (ATR) mode. The polymer was dried for 4 hours in a N_2 oven at 120 ^{o}C to prevent surface moisture from interfering with the spectrum. A background spectrum was collected for every run, and a total of 50 scans were averaged per sample.

X-ray photoelectron spectroscopy (XPS) was performed with a Thermo K-Alpha XPS spectrometer. High-resolution scans and depth profiles were collected using a 400 μm spot size of monochromated Al Kα X-rays with a 400 μm diameter spot size and a 1 mm raster size. Background pressure was maintained below 10^{-7} torr. The base pressure was 2×10^{-8} Torr, and the pressure within the chamber remained below 3×10^{-7} Torr throughout the experiments. The analyzer pass energy was set to 50 eV with a resolution of 0.05 eV and a dwell time of 100 ms. During these high-resolution XPS measurements, the sample was flooded with slow electrons and Ar+ ions using the flood gun to compensate for surface charging. Charge referencing was performed using the C 1s peak corresponding to C-C bond (284.8 eV) [121].

In situ XPS measurements were made tracking the chemistry as a function of chromium deposition. In accordance with the methodology reported by Wenzel *et al*.,[122] an L-shaped sample holder was used to allow for the sputter deposition of the Cr overlayers from a target. The holder is designed so that the Ar sputter gun within the XPS chamber can be used to deposit the target material. The holder features an 85° angle between the upright portion and the horizontal surface. The target material (Cr) was attached to the upright end of the holder using conductive carbon tape, and the sample was affixed to the horizontal surface of the sample holder 0.5 mm away from the target material (Cr). A chromium target was prepared by evaporating a ~300 nm thick film of Cr using an e-beam evaporator (Denton Explorer) onto a 4'' silicon wafer using a Cr source material (99.99% purity). The silicon wafer was then diced into 1 x 1 mm targets. These Cr targets were then in situ sputter deposited onto the polymer surfaces using Ar+ ions at an acceleration voltage of 3.0 keV and an ion current of 9.0 μA. The ion beam was rastered over a rectangular area of 4 × 2 mm. The angle between the horizontal sample and the sputter gun was 32°, and the sputter gun was directed at a position ~2 mm above the surface of the polymer. This resulted in sputtering of the target material in a cone-shaped plume, with the plume oriented to partially deposit onto the polymer.

High resolution XPS spectra were obtained from the region which corresponded to thickest Cr on the polymer. XPS spectra were collected after 0.5, 1, 1.5, 2, 2.5, 3, 6, and 9 min of Cr deposition.

A Shirley background was used for fitting XPS peaks in these experiments, and the peak shapes used were 70% Gaussian / 30% Lorentzian for all Mo 3d, S 2p, Li 1s, and Ge 3d peaks, while a Donjiac–Sunjic line shape was used for the asymmetric Ag 3d peak. For each high-resolution spectrum, the best fit for each data set was obtained as that with the minimum chi-square value.

Parallel-plate capacitance measurement:

A parallel plate capacitor test-structure was fabricated to measure the capacitance of VPI-treated and untreated polymer.

50nm Ti/ 150 nm Cu was sputtered on a 2" piece of silicon wafer. A 19 μm thick dry-film based BCB was partially vacuum laminated with 90 s of pulling vacuum and 60 s of hot press at 0.6 MPa into the substrate. The polymer was then cured at 250 °C for 1 hour . After curing, a single VPI sequence was carried out at 150 °C with a hold time of 5 hours. A metal mask was used to evaporate 450 nm of Al (Denton explorer 14 e-beam evaporator) to create square electrodes. The inter-layer capacitance of the control and the VPI-treated polymer was measured using an LCR meter. The electrode and the exposed Cu area on the wafer were used as the two probe points. Three measurements were taken across different electrodes.

5.2.2.3 Adhesion test:

Interfacial adhesion between the metal film and polymer was quantified using a 90° peel test (Testing Machines Inc. peel tester). Peel-tests were performed on 1-cm wide metal strips at a peel-rate of 30.5 cm/min. The substrate was carefully taped onto an FR-4 board which acted as a holder, which was then taped onto the peel test instrument to ensure that substrate warpage did not influence the measured peel

strength. The test setup is shown in Figure 56. Peel strength is dependent on three main factors: interfacial adhesion, bending angle of the delaminated film (for this case, copper), and elongation of the delaminated film. Controlling the thickness and uniformity of the plated copper ensures normalization of the second two factors such that comparisons can be made with respect to interfacial adhesion strength.

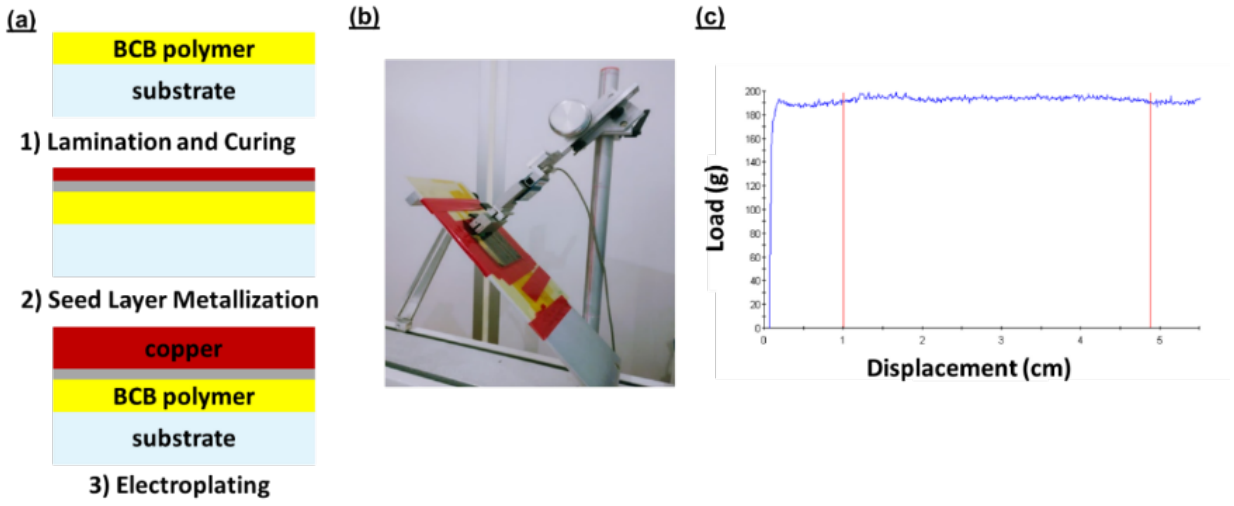
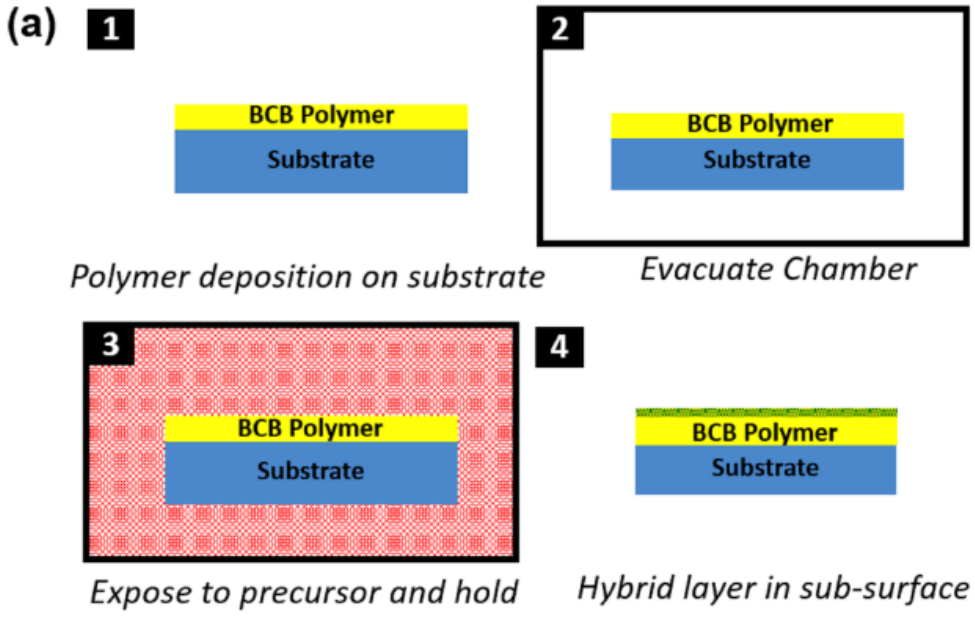


Figure 56 Schematic for the adhesion test (a) Process flow for peel test samples (b) TMI peel test and the sample arrangement (c) Typical load versus time/position graph where the average steady state value is taken as the peel strength

5.2.3 Results and Discussion

5.2.3.1 Chemical and Structural analysis:

Figure 57 (a) depicts the process flow for vapor phase infiltration. In this study we examine how VPI process temperature and time influence the adhesion of metal films to the polymer. The polymer chosen for this study, is a photo-sensitive dry-film BCB which is capable of supporting high-speed, high-density interconnects because of its inert low dielectric loss properties.



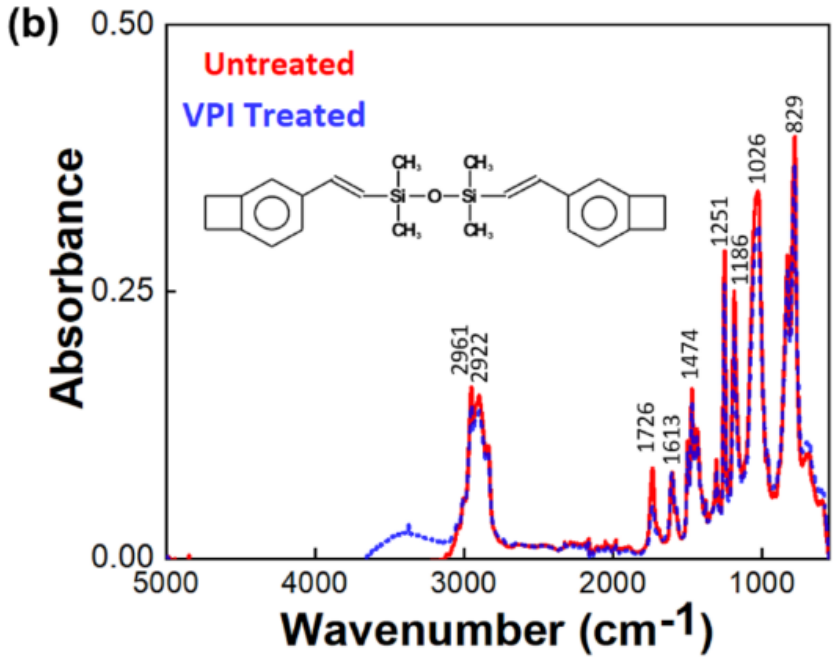


Figure 57 (a) Schematic of process flow for vapor phase infiltration (b) FTIR spectra of the Benzocyclobutene (BCB) polymer before and after TMA VPI treatment (150 °C, 6 hrs of TMA exposure)

Divinyl siloxane bis-Benzocyclobutene DVS-BCB is the pre-polymer which is dissolved in mesitylene and coupled with additives and crosslinkers to make it photo-sensitive and give it other desirable chemical properties. The siloxane linking groups give BCB excellent dielectric properties and low water absorptions due to their low polarizability. However, it is accompanied with drawbacks such as poor adhesion due to the non-polar structure. In this work, we seek to use the infiltration process to improve metal film adhesion. In our approach, we use a single dose of precursor to tailor the interfacial properties without affecting the bulk. Figure 57 (b) plots the FTIR spectrum collected from the BCB polymer before and after VPI treatment. The absorption bands shown in the spectrum correspond to the stretching vibrations typically seen for DVS-BCB [123]. These spectra are similar before and after VPI treatment. The only significant change is the appearance of a broad absorption between 3200 and 3700 cm^{-1}. This absorption is related to water or hydroxyls and is explored in the later sections. XPS C 1s scans as shown in Figure 58 further suggest minimal chemical changes to the BCB polymer upon VPI treatment.

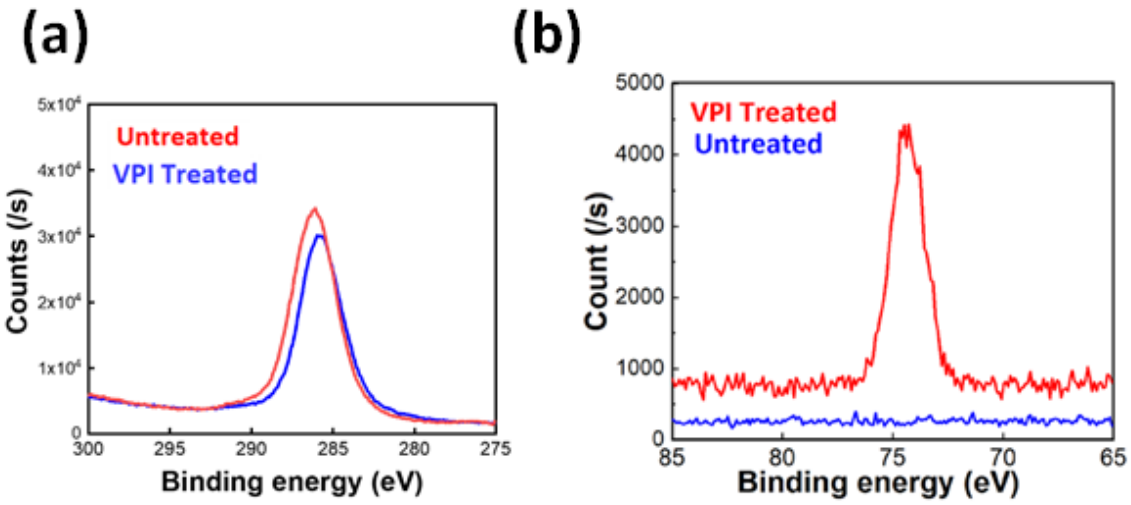


Figure 58 High resolution XPS (a) C 1s (b) Al 2p peaks of VPI-treated and un-treated BCB

Depending on the precursor and polymer selection and process parameters such as dose time, dose temperature, number of cycles, etc the precursor permeates through the polymer in different ways. For our

selection of a small precursor molecule, unreactive polymer with a large free volume we see no reaction between the precursor and the polymer, rather the precursor sorbs through the polymer reacts with the co-reactant and gets entrapped within the bulk of the polymer. To characterize the inorganic infiltration, we probed the VPI treated polymers with SIMS and XPS depth profile scans. Figure 59 summarizes the structural and chemical characterization of the polymer dielectric after AlO_x infiltration. This polymer underwent one VPI dose of TMA at 150 °C for 6 hours followed by a single water pulse. SIMS depth profile seen in Figure 59 (a) suggests that the aluminum oxide penetrates up to about 1.5 to 2 μm into the polymer's subsurface. The scan suggests that there is a higher concentration of Al at the top subsurface of the VPI-treated BCB. Water contact angle measurements were made to investigate the surface wetting characteristics. As shown in Figure 59 (b), the VPI-treated BCB polymers exhibits a significantly lower water contact angle, further confirming a chemical modification of the material.

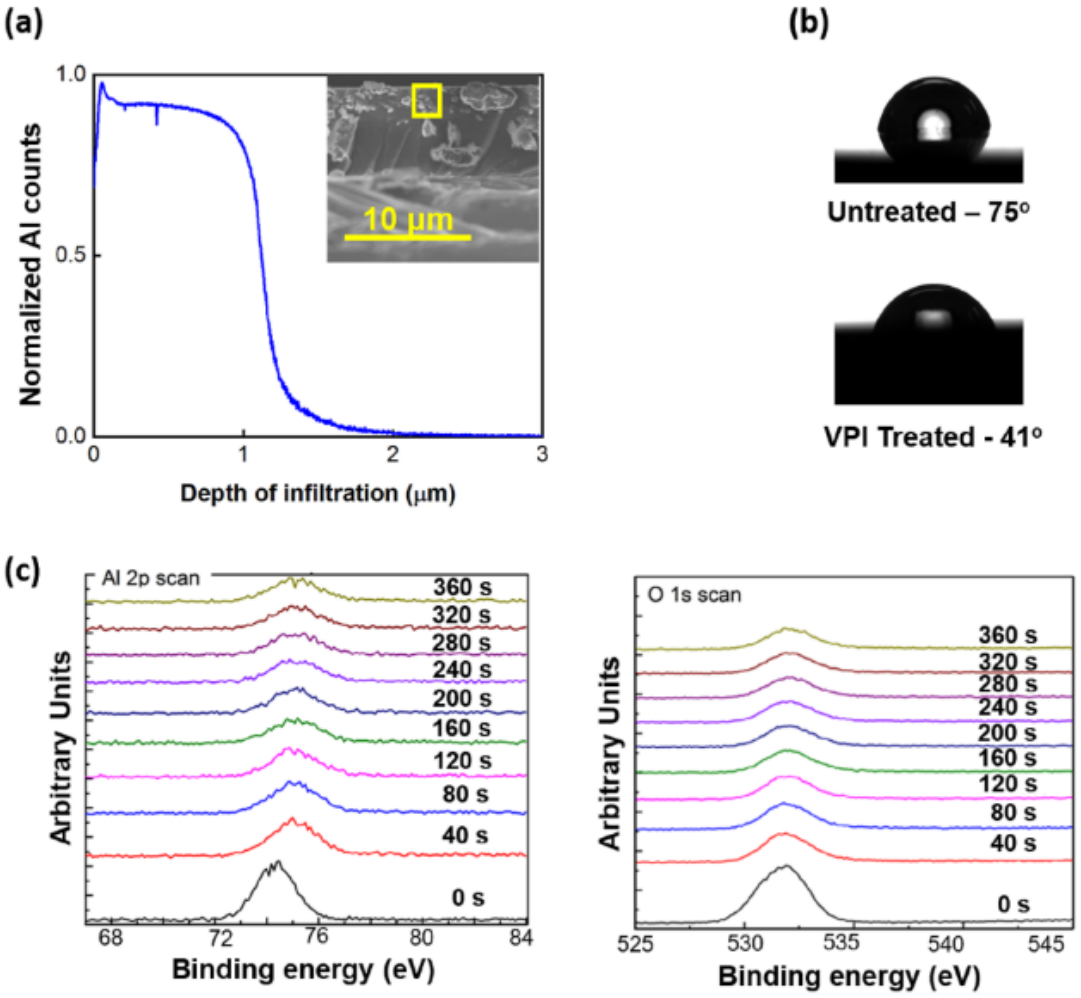


Figure 59 Chemical and structural characterization of VPI-treated BCB (a) Plot of normalized SIMS data for Al+ as a function of depth for an AlO_x infiltrated BCB polymer; inset: cross-sectional SEM image indicating the infiltrated depth versus the bulk of the polymer

Figure 59 (c) and (d) present depth profiles of high-resolution Al 2p and O 1s XPS scans collected from the AlO_x VPI treated BCB polymer. These plots show a series of XPS spectra collected from different depths using an argon plasma etch gun, which milled away consecutive layers of the material. Evident from this scan is the appearance of Al at the surface of the VPI treated polymer; prior to VPI treatment, no Al was detectable as seen in Figure 58 (b). We also observed a significant increase in the O

1s signal near the surface of VPI treated BCB compared to the bulk concentration, suggesting additional oxide content in the near surface of the treated polymer.

BCB-based polymer dielectrics are highly cross-linked polymers composed mostly of hydrocarbon and aromatic rings in a 3-dimensional network as shown in Figure 57. This hydrocarbon chemistry is generally unreactive towards metalorganic molecules like TMA [104]. For example, TMA is known to be unreactive towards polystyrene, although it will sorb and diffuse into the polymer and become entrapped if reacted with a co-reactant (e.g., H_2O) while still within the polymer [124-126]. The rigidity of this network also likely generates significant free volume for the diffusion of sorbed metalorganic precursors. Indeed, the inorganic infiltration is rather deep into the BCB considering the time and temperatures used. Previous work for PA-6 and PBT has shown an infiltration depth of < 1 μm for 10 cycles of single doses [127-129].

5.2.3.2 Adhesion Strength

Figure 60 summarizes the experimentally measured 90° peel testing adhesion strength for Cu/Cr films on BCB polymers that underwent VPI at varying process temperatures and infiltration times. Error bars represent the standard deviation from an average of 4-5 peels for each condition and the green band represents the average measured peel strength for the Cu/Cr film on untreated BCB (150 – 250 g/cm). Note that all of the VPI process temperatures are well below the polymer's glass transition temperature (250 °C). At lower process temperatures, interfaces trend towards greater adhesion strengths with longer infiltration exposure times. The highest adhesion strength was achieved at 150 °C with a 6-hour hold. This adhesion strength is more than twice the interfacial adhesion of the untreated BCB polymer. At the highest process temperature investigated (175 °C), adhesion strength remains low for all hold times with adhesion strength that are similar to the untreated polymer.

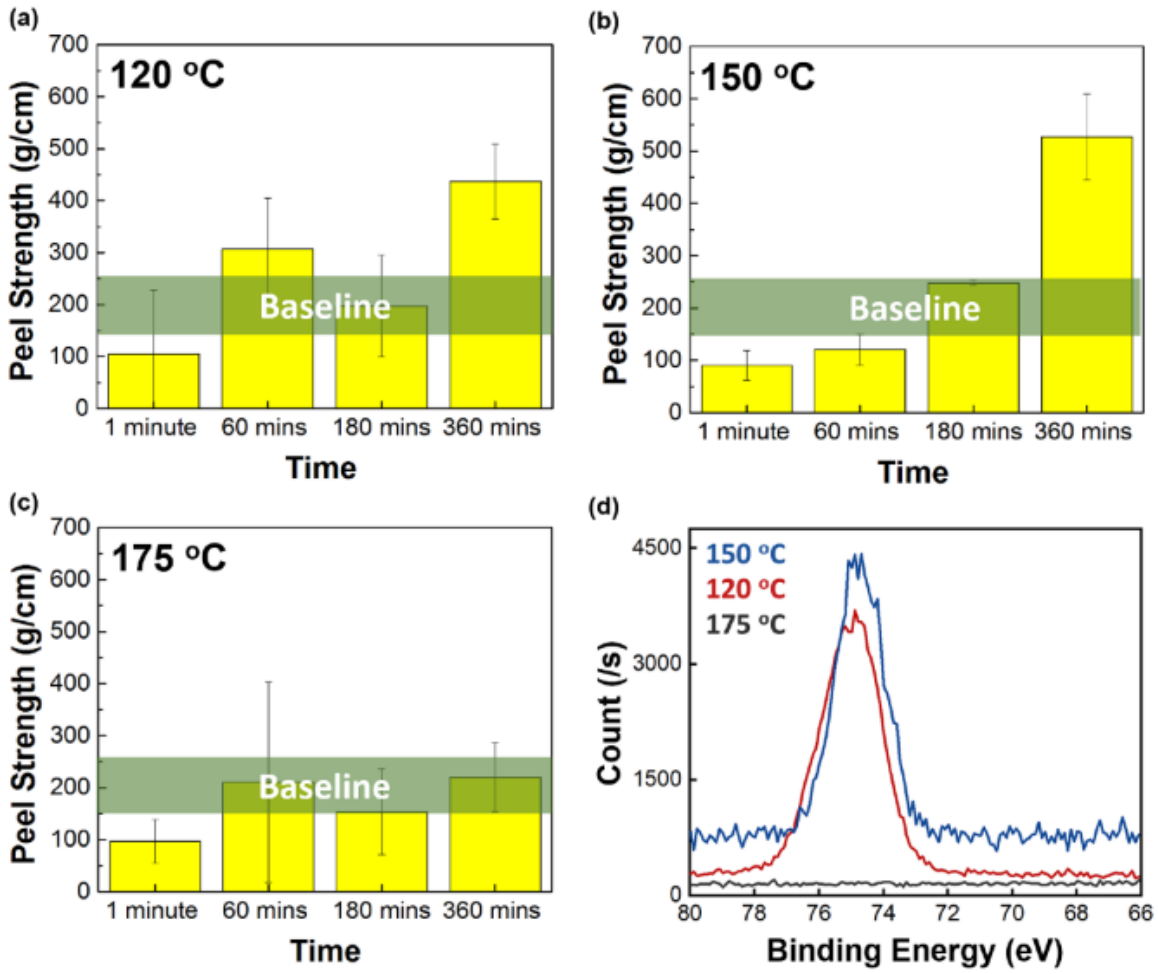


Figure 60 Averages of peel test measurements for adhesion strength between copper and BCB polymer for VPI-treated samples during different hold times using a single cycle VPI treatment. VPI temperature is (a) 120 °C (b) 150 °C (c) 175 °C. Green bands represent the average peel strength measured between copper films and untreated BCB polymers (control). (d) High-resolution XPS spectra of Al 2p, comparing VPI infiltration at different temperatures for the same duration

The reduced effectiveness of the VPI treatment at higher process temperatures may seem surprising. If the VPI treatment was simply reacting the metalorganic precursors with the polymer to form more covalent bonds at the interface, then it would be expected that at higher process temperatures the reaction rate kinetics would increase and adhesion strength would improve. The decline in adhesion strength with increasing process temperature suggests that a different mechanism is controlling interfacial adhesion.

Previously, Leng and Losego have shown that inorganic loading fraction decreases with VPI process temperature due to sorption thermodynamics [130]. At higher process temperatures, sorption of metalorganic vapors into the polymer is less favorable because the condensation step is an exothermic process. In Figure 60 (d) we confirm using a high-resolution Al 2p XPS scan that AlO_x loading drops precipitously at the VPI processing temperature of 175 °C. This lack of chemical modification at higher VPI temperatures leads to a less effective adhesion "layer". If higher temperatures were desired to accelerate diffusion kinetics and reduce the 6-hour infiltration time, it may be possible to offset this loss in loading by using higher precursor partial pressures.

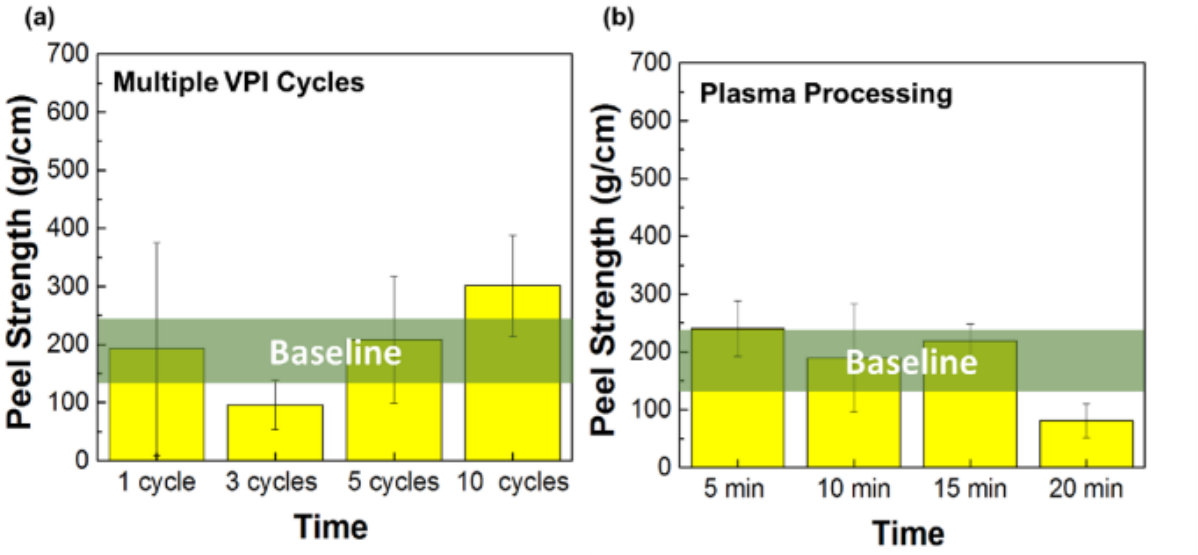


Figure 61 Average of peel test measurements for adhesion strength between copper and BCB polymer using (a) multiple VPI cycles with 1 minute holds (b) argon plasma treatments of BCB films for varying times. All VPI treatments were carried out at 150 °C.

We next examined another approach to increasing inorganic loading, using multiple VPI exposure cycles, or what is sometimes called sequential infiltration synthesis (SIS) [106, 131, 132]. Figure 61 (a) summarizes the peel strength after multiple infiltration doses. Here we chose to use short infiltration times to limit the depth of inorganic infiltration. One cycle consisted of a 1 s TMA dose (<~1 Torr) / 60 s static

pressure hold / 1 s H_2O dose / 90 s purge. All infiltration sequences were executed at 150 °C since this temperature provided the highest adhesion strength in the prior experiment (Figure 60). As shown in Figure 61 (a), these interfaces also showed a general trend towards higher interfacial strength with more VPI cycles. However, this improvement is mostly within measurement error and never becomes as significant as the longer hold times. We are also uncertain as to why in some cases we appear to detect a decrease in adhesion strength at low exposure times and cycle numbers. Al 2p high-resolution XPS depth profiles of short, multiple exposure sequences are compared with single long doses in Figure 62 and we see that the short exposures do not see deep infiltration depth. Perhaps the short exposures lead to some sort of degradation via, e.g., humidity, that reduces strength modestly prior to the improvement that is eventually achieved with deeper and higher concentrations of inorganic loading. Regardless, this data suggests that longer hold times leading to deeper infiltration depths are likely important to improving adhesion. Even with multiple cycles, adhesion is not improved if the infiltration time is low and the depth is shallow.

To further investigate the impact of near surface chemical modifications, we also considered plasma treatments. Based on literature reports [43] argon plasma provides better adhesion to BCB than oxygen plasma; the latter tends to oxidize the polymer and weaken bonding to the metal. The BCB polymers were exposed to an Ar plasma RIE for 5 min, 10, 15 min, and 20 min. As shown in Figure 61 (b) peel strengths remained relatively constant with plasma treatment up to 15 min of exposure, with most interfacial adhesion strengths within the range of the control, untreated BCB polymer.

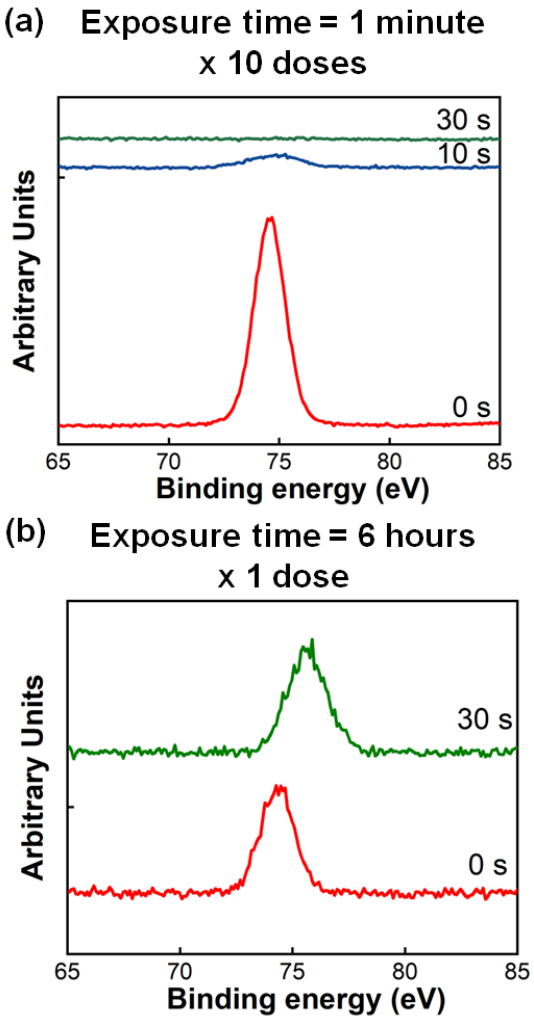


Figure 62 (a) Depth profile of high-resolution Al 2p XPS scan at 0 s, 10 s and 30 s of argon sputter time. The infiltration is done at a hold time of 1 minute at 150 °C for 10 doses of TMA. (b) Depth profile of high-resolution Al 2p XPS scan at 0 s and 30 s of argon sputter time. The infiltration is done at a hold time of 6 hours at 150 °C for 1 dose of TMA.

5.2.3.3 Adhesion mechanism

To better understand the nature of the interfacial fracture, we probe the chemistry of both sides of the peel interface after the peel test. A representative peel sample is shown in Figure 64 along with the fractography surfaces of the baseline control sample in Figure 63 (a). XPS analysis of the untreated BCB fracture surface reveals primarily Cr/Cu on the peel side and primarily C on the substrate side. As depicted

below these spectra, this result suggests that fracture occurs at the metal/polymer interface. In contrast, XPS analysis of the optimized VPI treated BCB fracture surface (150 °C, 6 hrs of exposure) reveals significant carbon on both the peel side and the substrate side as shown in Figure 63 (b). This result is indicative of cohesive bulk fracture within the polymer, suggesting the interface is now stronger than the polymer itself. This shift in the failure interface indicates that the interfacial bonding achieved after VPI treatment is the strongest possible for the polymer. Further, the Al 2p/Cr 3s peak on the peel side of the VPI-treated BCB fracture surface suggests that the interfacial failure occurs in the polymer bulk.

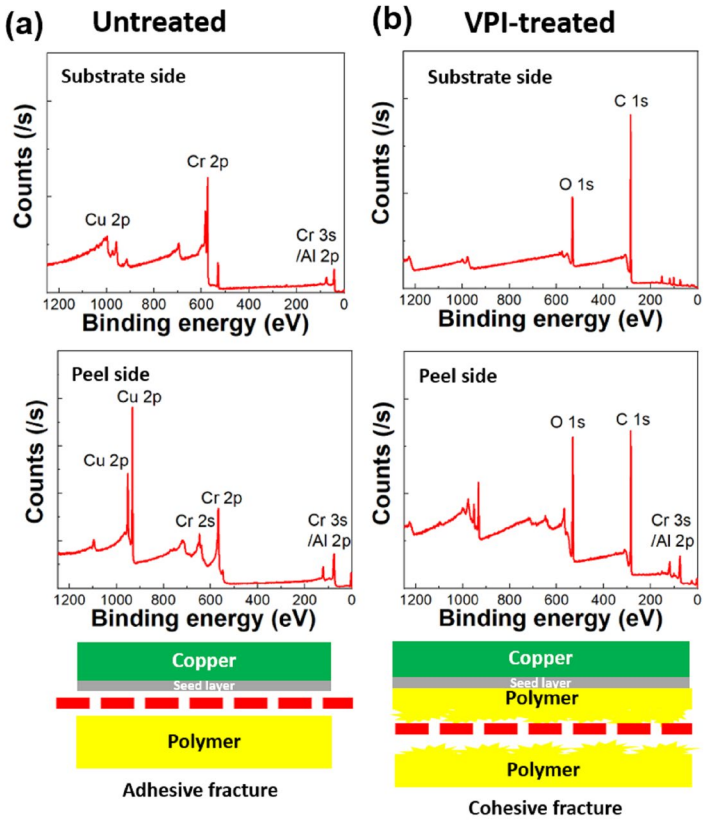


Figure 63 (a) XPS data collected from the fracture surfaces of a metal film deposited on an untreated BCB polymer; (b) XPS data collected from the fracture surfaces of a metal film deposited on a BCB polymer infiltrated with AlOx. Diagrams below the XPS data show our interpretation of where fracture is occurring in each of these systems.

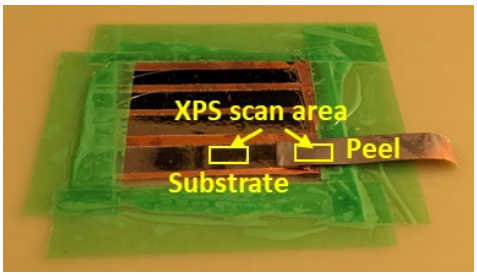


Figure 64 Photograph of a peeled copper film showing how the fracture surface of both the "peel side" and "substrate" side can be examined.

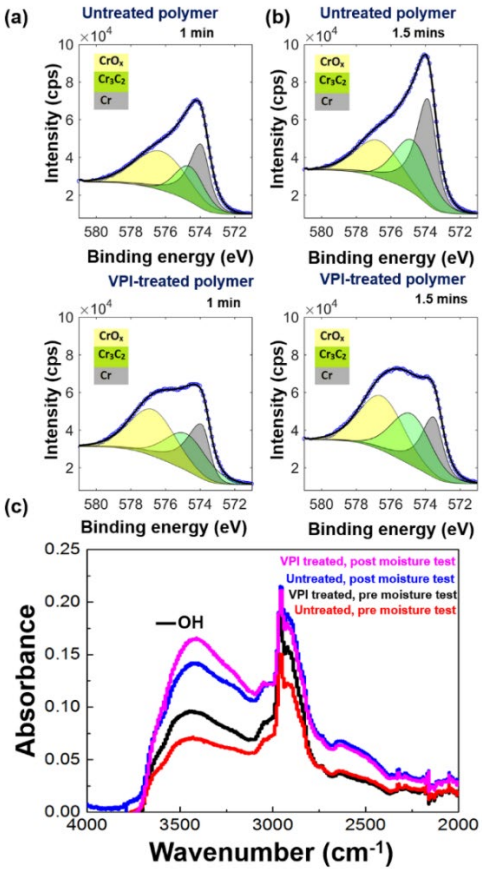


Figure 65 (a) High resolution XPS spectra of Cr 2p with progressive deposition of metal on untreated and TMA infiltrated BCB polymers (150 ºC, 6 hours); (a) 1 minute of sputter time (b) 1.5 mins of sputter time; (c) FTIR spectra for untreated and TMA infiltrated BCB polymers (150 oC, 6 hours) held in a dry environment and then exposed to a humidity chamber test (130 ºC, 85%RH, 24 hours).

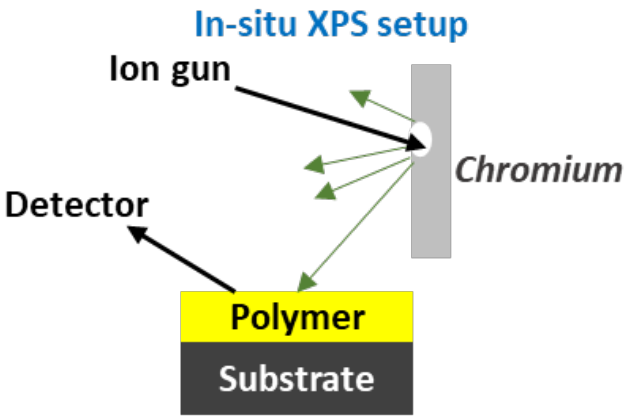


Figure 66 Schematic setup for the in-situ XPS.

We also sought to understand whether the infiltration modified the interfacial reactions between the chromium seed layer and the polymer surfaces. We probed the interface using a custom experimental testing rig shown in Figure 66 that allows us to collect XPS spectra while depositing the first few nanometers of the Cr adhesion layer. Figure 65 compares the high-resolution Cr 2p XPS spectra after (a) 1 min and (b) 1.5 min of Cr deposition on untreated and VPI-treated (150 °C, 6 hrs) BCB polymer. Evident in these spectra is a greater prevalence for chromium oxide in the films deposited on VPI treated BCB polymer. This presence of additional CrO_x at the interface may be further contributing to the improved adhesion. We believe this increased reactivity may be a confluence of multiple factors. First, we detected more oxygen near the surface of VPI treated BCB, so the Cr may just be reacting with the AlO_x present. Second, we suspect that the AlO_x BCB is more hygroscopic than the untreated polymer. These sorbed water molecules may be desorbing during the sputtering process resulting in more oxidation of the depositing Cr film. To provide additional evidence of this potential water content, we examined the FTIR spectra of the treated and untreated BCB polymers before and after exposure to a high humidity environment (130 ºC, 85% RH for 24 hours). These FTIR spectra are plotted in Figure 65 (c). The -OH spectral band in the 3200 – 3700 cm^{-1} region is more intense in the VPI-treated BCB films both before

and after humidity exposure. This observation further suggests that sorbed water may be contributing to the Cr oxidation.

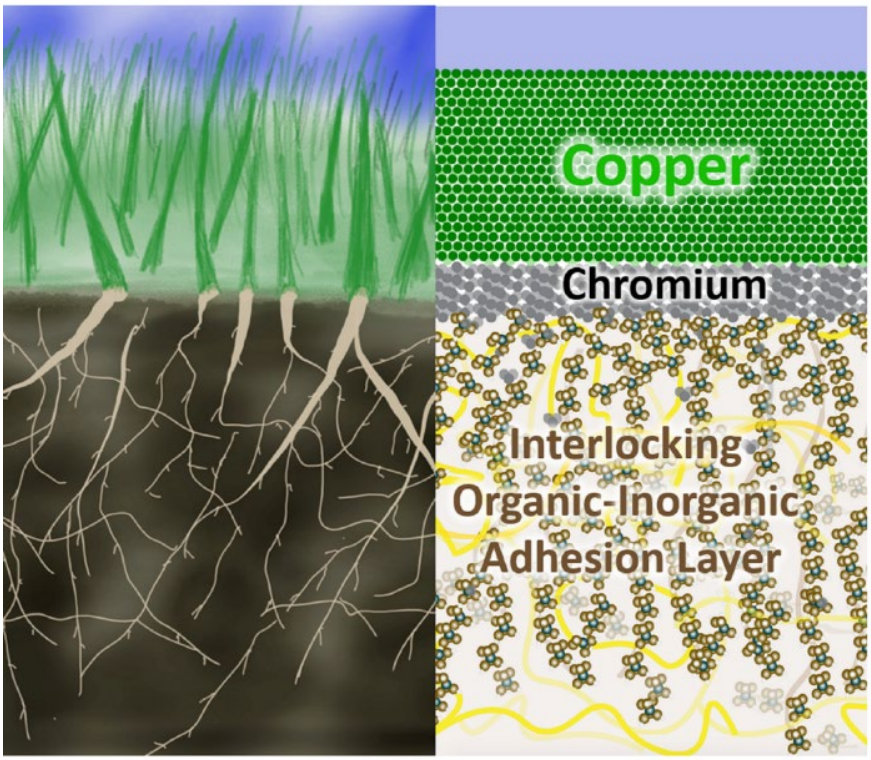


Figure 67 Schematic showing the proposed mechanism for adhesion enhancement. Infiltrated inorganics (molecular units) form an interpenetrated network with the organic chains (yellow lines) within the subsurface of the polymer. This organic-inorganic interlocking forms a root structure, with the inorganic portion forming strong chemical bonds to the overlying metal layers, anchoring them to the polymer. Conceptually, this mechanism is similar to the root system that anchors plants to the soil.

Based on the above observations, we propose that the enhancement to interfacial adhesion observed here is likely a combination of the infiltrated inorganic interlocking with the polymer chains and forming a strong chemical bond to the subsequently sputter deposited Cr/CrO_x adhesion layer. While the AlO_x appears to be uniformly distributed throughout the polymer subsurface, we cannot find any evidence for direct chemical bonding between the inorganic and the polymer. This is consistent with other observations with non-polar polymers such as Teflon which do not have functional groups to react with the infiltrate

but use physical entrapment to lock in the inorganics[133]. This lack of bonding suggests that the mechanical interweaving of the inorganic and polymer chains is sufficient to provide mechanical interlocking of the two materials. As pictured in Figure 67 , we envision this subsurface network of AlO_x as an inorganic "root-like" system that is difficult to mechanically remove from the polymer. Near the surface, AlO_x units readily form chemical bonds to the deposited chromium layer, which then metallically bonds with the copper film. Consistent with this model is the time at temperature necessary to "grow" a root system that is deep enough and interconnected enough to be well interlocked with the polymer chains.

Finally, we did preliminary testing on the changes in dielectric properties of the BCB polymer before and after infiltration. These tests consisted of capacitance measurements in a parallel plate geometry with the untreated and treated BCB as the dielectric layer. Exact test procedures are included in the SI. The measured capacitance value for the un-treated BCB polymer is found to be 23.06 + 0.46 pF at 100 kHz. The AlOx infiltrated polymer has a capacitance of 23.08 + 0.23 pF at 100 kHz. Thus, no significant change in dielectric properties is detected within our measurement error. This agrees with our model of the VPI treatment only modifying the sub-surface and not significantly altering the bulk polymer chemistry or properties.

5.2.4 Summary:

Vapor-phase-infiltration was used to achieve 3x improvement in metal/polymer interfacial adhesion strength. Key process parameters such as time and temperature must be controlled to to achieve optimal adhesion. When optimized, the failure mechanism appears to shift from metal/polymer interfacial delamination to cohesive failure of the bulk polymer. Chemical characterization indicates that the VPI process infuses inorganics into the polymer to a depth of at least 2 μm. These reactions also generate increased oxygen and sorbed water content near the polymer's surface. These species increase the VPI

treated polymer's reactivity with sputter deposited metal adhesion layers like chromium. Because VPI has a low thermal budget and large-area scalability, this approach for chemically improving the adhesion to a non-polar polymer is compatible with most microelectronics packaging fabrication processes and we expect it to find broad applicability to a range of dielectric build-up films and mold compounds with adhesion challenges.

5.3 Chapter summary

This chapter focuses on two critical reliability aspects for high-density ultra-low D_k, ultra-thin polymer RDL (a) thermo-mechanical reliability of the copper/polymer interface (b) chemical or interfacial adhesion reliability of copper/polymer interface. The first section evaluates the effect of dielectric material properties on RDL reliability. The critical test-structure identified was a microvia with < 5 μm diameter to understand the impact of polymer dielectric material properties on the fatigue strains at the via/pad interface. A finite-element modeling (FEM) approach was used to predict the influence of CTE and modulus on the overall TCT reliability. A daisy-chain test-structure was fabricated and characterized for TCT reliability. The failure mechanism of via cracking at the pad/via interface matches the modeling predictions. The number of cycles to failure of 1700 falls within the window of 1470 and 1930 predicted by the FEM simulations. This work presents guidelines to design reliable <5 μm diameter microvias and provides a fundamental insight into the effect of polymer properties on microvia reliability. The residual stress that polymer RDL imparts on the substrate at different stages in processing was studied. The polymer CTE and modulus play a dominant role with the initial stress being influenced by the polymer structure. During high-temperature annealing steps is when the polymer RDL develops maximum stress. This stress can be minimized by using a low-CTE, low-modulus dielectric material and maintaining processing temperatures below a maximum limit. The second section investigates a novel polymer sub-surface modification technique to its' applicability in improving interfacial adhesion for an ultra-low D_k

material candidate. Vapor-phase-infiltration (VPI) was used to improve interfacial adhesion by 3X for BCB. A processing window for the process was identified after conducting a time-temperature optimization. Extensive chemical and structural characterization were done to understand the effect of VPI on the polymer structure and the results demonstrate an infiltration of <1.5 μm with no change to the base polymer chemical structure and dielectric properties of BCB. This work demonstrates the creation of a hybrid inorganic-organic sub-surface that consists of interpenetrating inorganic molecules in the polymer chain which bond to the metal deposited and improve adhesion.

CHAPTER 6. SUMMARY AND FUTURE WORK

This dissertation presents a comprehensive study on solutions to critical challenges associated with ultra-thin, ultra-low D_k polymer dielectrics for next-generation high-density RDL. Silicon back-end-of line (BEOL) RDL has significant limitation such as high RC delays because of the choice of dielectric materials and cost and thus, is challenged in terms of meeting the bandwidth requirements for future AI driven high-performance and edge-computing applications. Current organic materials and processes are limited by their potential to scale to fine features by thick dielectric materials and poor dimensional stability of the core. This research demonstrates the potential for ultra-low D_k , ultra-thin polymer dielectrics to signal at higher data rates, process guidelines for panel-scalable and low-cost processes to deposit ultra-thin dielectrics and evaluates reliability of ultra-thin, ultra-low D_k dielectrics, thus leading to enhanced electrical performance and lower cost compared to silicon BEOL and current organic RDL.

6.1 Research summary

The primary objective of this research is to develop ultra-low D_k, ultra-thin polymer dielectric materials, processes and reliability to meet next generation interconnect needs for ultra-high bandwidth. The research was focused on three key areas (a) Ultra-low D_k polymer dielectric materials (b) Ultra-thin polymer dielectric processes, and (c) Ultra-low D_k, Ultra-thin dielectrics thermo-mechanical and chemical reliability.

6.1.1 Ultra-low D_k polymer dielectric materials:

The fundamental need for this work is because current dielectrics do not meet the ultra-low D_k target and cannot support data-rates needed for next-generation ultra-high bandwidth. The research task defined to address this challenge is to evaluate ultra-low D_k materials and identify material classes

depending on polymer structure and property and characterize performance improvement with low D_k materials for high-speed signaling. This research identifies epoxy, BCB and phenolic resin as potential dielectrics based on their electrical, physical, mechanical and chemical properties. Epoxies are the workhouse material for packaging substrates because they offer an optimal property window, however they do not meet the electrical ultra-low D_k requirements for this research. In order to push the boundaries beyond epoxies, BCB and phenolic resin material classes were identified as having material properties capable of improving electrical performance while being processable using panel-scale process to fabricate fine-pitch structures with reliable interfaces. Further, test-structures were designed and characterized to demonstrate signaling potential > 4.8 Gbps for ultra-low D_k materials achieving a bandwidth improvement of 35% over silicon BEOL RDL. These materials were tested for insulation reliability before and after HAST and demonstrated no significant increase in leakage current, proving their potential to meet next generation needs. Thus, this chapter identifies and characterizes advanced materials capable of meeting next-generation high-density RDL needs for ultra-high bandwidth.

6.1.2 Ultra-thin polymer dielectric processes

Current processes cannot support high RDL density across panel-scale with ultra-thin dielectrics. The research task identified to address this challenge is to develop panel-scalable ultra-high density RDL processes for ultra-thin, ultra-low D_k dielectrics with least DoP. In this work, fabrication of fine-pitch features using semi-additive processing (SAP) is discussed in detail and process limitations for ultra-thin dielectrics. Representative dry-film and liquid dielectric material candidates are selected, and a DoE is conducted to study the effect of feature-size and process conditions on the surface planarity. This study describes a methodology and critical processing parameters required to achieve high surface planarity for fine-pitch features. Vacuum time and pressure were identified as critical steps in the two-stage vacuum lamination process used to planarize the surface. The surface planarity of fine-pitch dry-film based

dielectrics was maintained < 5 μm. For liquid dielectrics, an additional fly-cut planarization step was needed to achieve < 5 μm planarity, particularly for tall copper features.

6.1.3 Ultra-low D_k and Ultra-thin polymer dielectric reliability

The critical thermo-mechanical and chemical reliability challenges associated with advanced dielectrics are a) ultra-thin dielectrics increases RDL stress, and b) ultra-low D_k materials are non-polar and have poor adhesion to copper. This dissertation identifies two tasks to address the reliability challenges a) evaluate effect of dielectric material properties on RDL reliability, and b) investigate surface modification techniques to improve adhesion. For the first task, this thesis evaluates the effect of polymer CTE and modulus on RDL reliability. For vertical interconnects, an FEM-based approach is used to predict the effect of these properties on the fatigue strains in copper. A daisy-chain test-vehicle is designed and fabricated to correlate the experimental results to simulation predictions. The TCT reliability for a 3 μm diameter via with a material candidate of interest is studied and the failure of 1700 falls within the range predicted by the thermo-mechanical simulations. The residual stress for lateral interconnects is studied and the effect of processing parameters on the development of stress is analysed. During high temperature processing steps, the cool down process builds in stresses within the RDL because of material property mismatch between the polymer and copper. For the second task, a unique approach is used to modify the subsurface of the ultra-low D_k dielectric to create an interlocking structure of hybrid organic-inorganic molecules that entraps the metal deposited and improves adhesion by 3X. Chemical and structural characterization was carried out to show infiltration up to < 1.5 μm of the polymer and increased hydrophilicity. An optimal processing window of time and temperature was found for VPI of BCB using TMA and H_2O as co-reactants. A fundamental interfacial adhesion mechanism was proposed using XPS and FTIR studies. This demonstrates the first application of vapor-phase-infiltration (VPI) as a processing technique of great interest in packaging substrates to improve interfacial adhesion.

6.2 Technical and Scientific Contributions

This research has advanced one of the critical focus areas in substrate packaging by improving dielectric materials and paving a path for ultra-low D_k, ultra-thin polymer dielectrics. It has evaluated in detail several key challenges and presented manufacturable solutions to address them. In particular,

- Design, fabrication and characterization of next-generation high-density RDL using ultra-low D_k, ultra-thin dielectrics to achieve ultra-high bandwidth
- Fundamental material structure-electrical performance correlation to evaluate all dielectric material classes and presents a guideline for material selection
- Developing and optimizing a process window for a planar surface using ultra-thin liquid and dry-film dielectrics on an SAP-based process flow
- Thermo-mechanical reliability and predictive modeling of the effect of polymer CTE and modulus on the strains in a < 5 μm diameter microvias for high-density RDL
- Developed a novel vapor-phase-infiltration technique to improve the interfacial adhesion of ultra-low D_k polymer to copper

6.3 Future work

This research suggests the following points of extension for further development of ultra-low D_k, ultra-thin polymer dielectrics and extend advanced RDL technology:

- This work has characterized material properties for high-performance computing applications. There is increasing interest in evaluating material properties in the THz frequency range and developing materials with stable properties in this frequency range.

- This work looks at surface planarity affected by the dielectric material and feature size. Additional investigations have to be performed in demonstrating planarity for multi-layer (2 or more) fine-pitch RDL with advanced ultra-low D_k, ultra-thin dielectrics. The process of fly-cut planarization needs to be better understood in terms of the effect of spindle speed and adhesion of different dielectrics.

- The VPI process conditions identified in this thesis involve long times of high-temperature processing. Additional investigations can be performed on identifying other precursors or increasing the partial pressure of the precursor to improve infiltration at a shorter time.

- VPI adhesion mechanism indicate a correlation between the depth of infiltration and adhesion strength, as shorter cycles do not significantly increase the adhesion strength. Additional investigations to study the minimum depth required for higher adhesion strength can be performed.

- The semi-additive process is limited in extending to < 1 μm line widths/spaces because of the critical challenge in the seed-layer etch chemistry destroying the structural integrity of the ultra-fine-pitch lines. There needs to be work on dry-etch of the seed-layer to improve RDL yield.

- There has been work in progress on inorganic coatings such as silicon nitride and organic coatings such as paralyene as a barrier layer for electrochemical migration however these coatings are >0.5 μm. Ultra-thin ALD coatings can be considered as barrier layers to create enhanced RDL structures which passive the copper lines.

APPENDIX: MICROVIA RELIABILITY

Table 14 Summary of DoE for microvia reliability

Trial number	Aspect ratio (AR)	Coefficient of thermal expansion (CTE)	Young's modulus (Y)	Via diameter	Total strain range (TSR)
1	1	30	1.5	2	0.0142
2	1	30	1.5	3	0.00392
3	1	30	1.5	5	3.07E-04
4	1	30	3	2	0.017
5	1	30	3	3	0.0083
6	1	30	3	5	0.00215
7	1	30	7.5	2	0.0183
8	1	30	7.5	3	0.0118

9	1	30	7.5	5	0.00877
10	1	45	1.5	2	0.0326
11	1	45	1.5	3	0.0207
12	1	45	1.5	5	0.00365
13	1	45	3	2	0.0336
14	1	45	3	3	0.0246
15	1	45	3	5	0.017
16	1	45	7.5	2	0.0354
17	1	45	7.5	3	0.0276
18	1	45	7.5	5	0.0232
19	1	60	1.5	2	0.0527
20	1	60	1.5	3	0.0385

21	1	60	1.5	5	0.0196
22	1	60	3	2	0.0498
23	1	60	3	3	0.0393
24	1	60	3	5	0.0318
25	1	60	7.5	2	0.0536
26	1	60	7.5	3	0.0444
27	1	60	7.5	5	0.0382
28	1.67	30	1.5	2	0.0123
29	1.67	30	1.5	3	0.00897
30	1.67	30	1.5	5	0.00573
31	1.67	30	3	2	0.0127
32	1.67	30	3	3	0.0102

33	1.67	30	3	5	0.00768
34	1.67	30	7.5	2	0.0135
35	1.67	30	7.5	3	0.013
36	1.67	30	7.5	5	0.00996
37	1.67	45	1.5	2	0.0234
38	1.67	45	1.5	3	0.0182
39	1.67	45	1.5	5	0.0143
40	1.67	45	3	2	0.0296
41	1.67	45	3	3	0.0215
42	1.67	45	3	5	0.0189
43	1.67	45	7.5	2	0.0301
44	1.67	45	7.5	3	0.0283

45	1.67	45	7.5	5	0.0226
46	1.67	60	1.5	2	0.0442
47	1.67	60	1.5	3	0.0294
48	1.67	60	1.5	5	0.0252
49	1.67	60	3	2	0.0436
50	1.67	60	3	3	0.0343
51	1.67	60	3	5	0.0319
52	1.67	60	7.5	2	0.0481
53	1.67	60	7.5	3	0.0446
54	1.67	60	7.5	5	0.0361

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